



Analog Reinvented

# ES9017 32-bit High-Performance 8-Channel DAC Product Datasheet

The ESS Sabre® ES9017 is a 32-bit 8 Channel digital-to-analog converter (DAC) that has the best cost/performance solution for receivers, personal audio devices, professional audio applications such as recording systems, mixer consoles and digital audio workstations (DAW) audio processors applications. It was designed to complement the new generation of the world's highest performing audio PRO DAC series.

The ES9017 has 8 integrated DACs which use ESS' new patented Hyperstream® IV DAC Architecture. The same technology that is used in the ESS Sabre PRO lineup. It delivers incredible audio sound quality and specifications, including +120dB DNR and -110dB THD+N per channel.

The ES9017 SABRE® DAC improves on previous designs to include:

- TDM & SPI support for more options in connectivity
- Lower power consumption than previous generations, including the Hyperstream® IV DAC modulator
- New Hardware mode for simplified programming.

TDM, DSD, DoP, and I2S, LJ, RJ, master/slave interfaces are supported.

The ES9017 has 7 built-in pre-programmed digital filters which allows the most discerning user to tune the SABRE® sound to their own personal sound signature.

FEATURE	DESCRIPTION
Patented 32-bit HyperStream® IV Architecture DAC Technology	32-bit audio DAC with high dynamic range & ultra-low distortion
+120db DNR per channel -110dB THD+N per channel	Excellent dynamic range and low distortion
High Sample Rates	Up to PCM 768kHz & native DSD512
Customizable filter characteristics	7 predefined digital filters, optimized for latency or sound color
Multiple Input formats are available	TDM, I2S, LJ, RJ, DSD, DoP
I2C, SPI, and Hardware interface control	Configured by microcontroller or other I2C/SPI source, or pins through Hardware Mode
Lower Power Consumption than Previous Gen	Simplifies power supply design
Standardized Packaging	7mm x 7mm, 48 pin QFP and 48 QFN for reduced PCB board space
Patented 32-bit HyperStream® IV Architecture DAC Technology	32-bit audio DAC with high dynamic range & ultra-low distortion

## APPLICATIONS

- Digital audio workstations (DAW) Audio Playback
- A/V Receivers (AVR)
- Personal Audio Devices & Media Streamers
- Sound Bars
- Mixers
- High End Audio Equipment
- DAP (Digital Audio Players)
- DJ Equipment



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### Functional Block Diagram

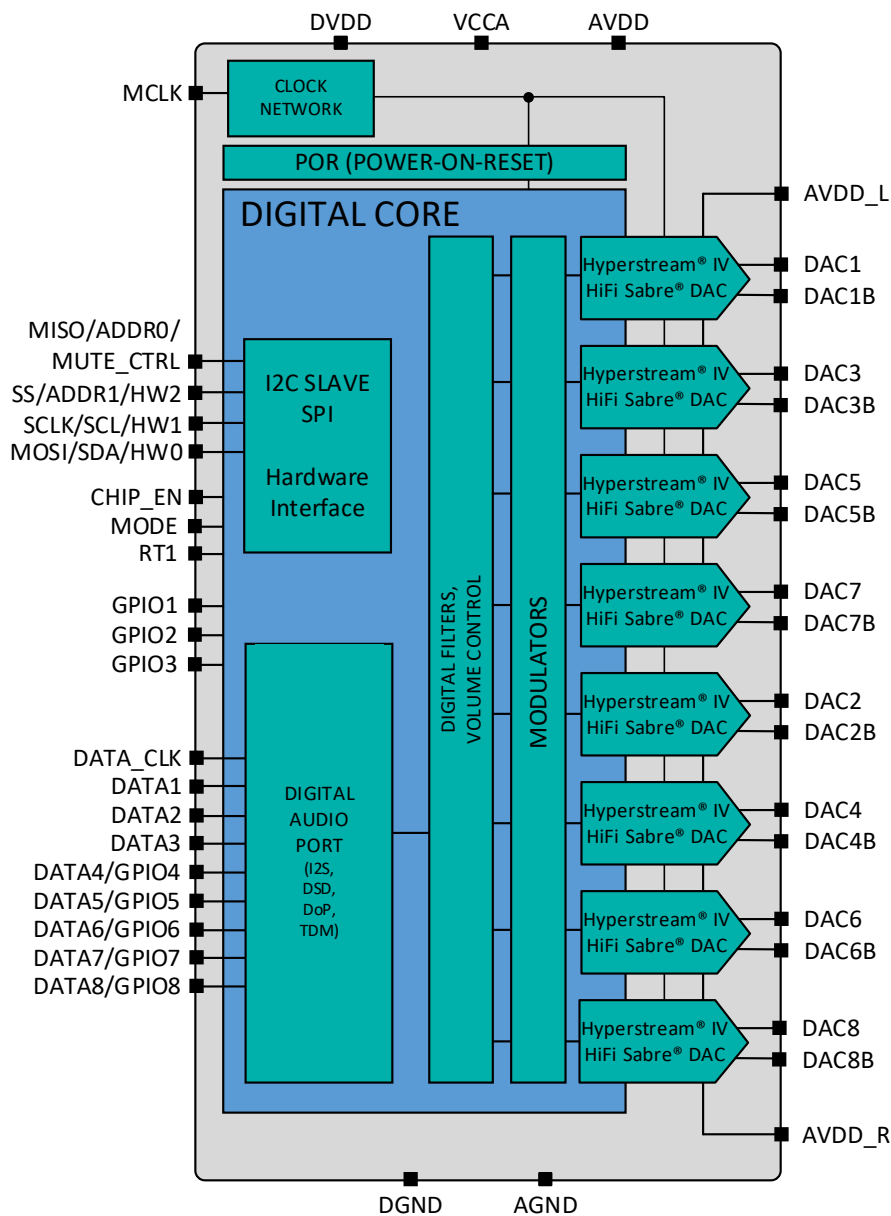
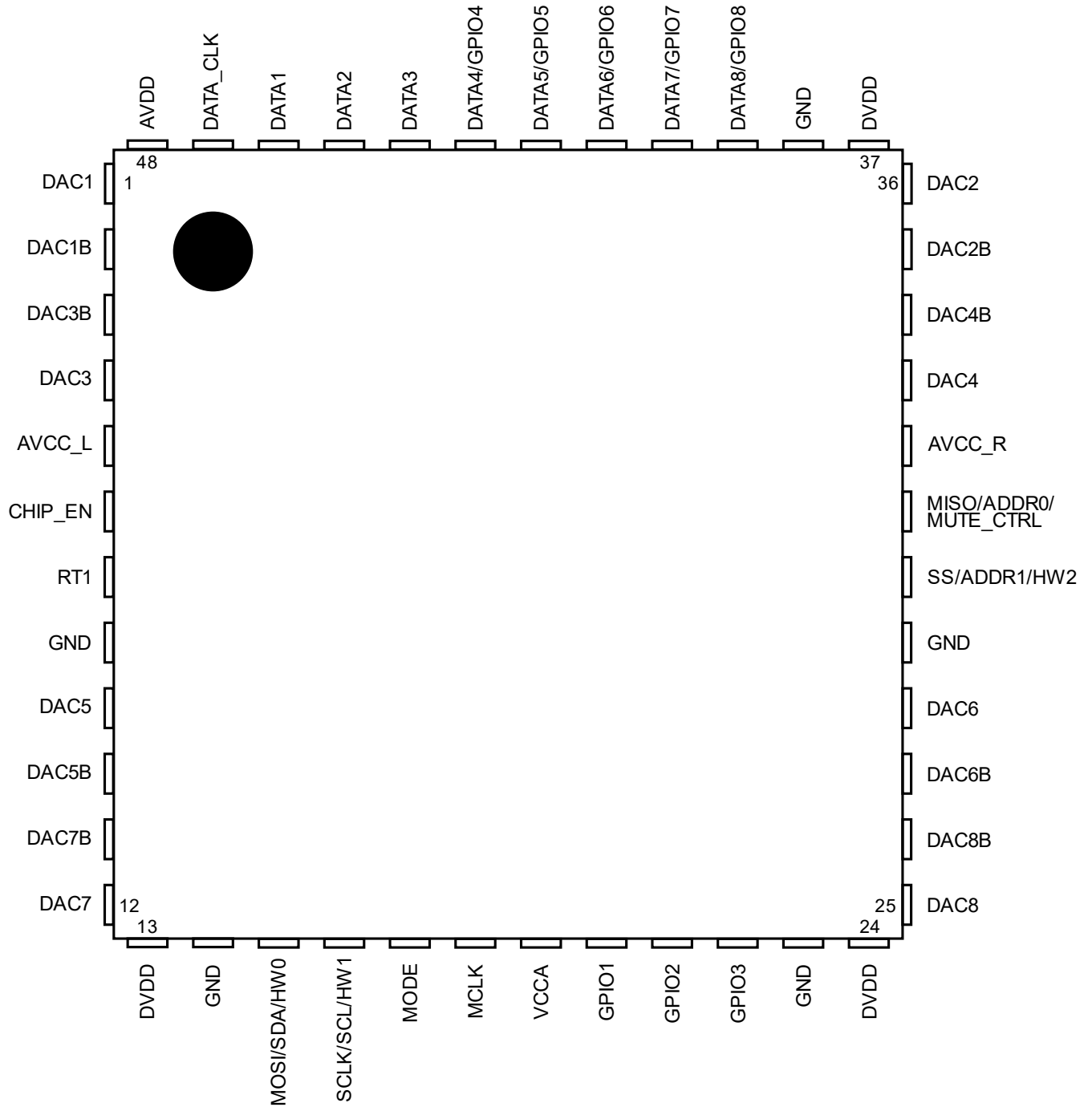


Figure 1 - ES9017 Block Diagram

ES9017 Pinout

48 QFN/QFP Pinout



ES9017S & ES9017Q Pinout\*  
(Top View)

\*Note: ES9017Q has an exposed pad (pin 49) that should be connected to ground, ES9017S does not have an exposed pad.



## 48 QFP/QFN Pin Descriptions

Pin	Name	Pin Type	Reset State	Pin Description
1	DAC1	AO	Ground	Differential Positive Output for Channel 1
2	DAC1B	AO	Ground	Differential Negative Output for Channel 1
3	DAC3B	AO	Ground	Differential Negative Output for Channel 3
4	DAC3	AO	Ground	Differential Positive Output for Channel 3
5	AVCC_L	Power	Power	3.3V DAC analog output stage reference supply for the Left side
6	CHIP_EN	I	HiZ	Active-high Chip Enable
7	RT1	I	HiZ	Reserved. Must be connected to DGND for normal operation.
8	AGND	Ground	Ground	DAC analog output stage ground
9	DAC5	AO	Ground	Differential Positive Output for Channel 5
10	DAC5B	AO	Ground	Differential Negative Output for Channel 5
11	DAC7B	AO	Ground	Differential Negative Output for Channel 7
12	DAC7	AO	Ground	Differential Positive Output for Channel 7
13	DVDD	Power	Power	Digital Core Supply, 1.2V
14	DGND	Ground	Ground	Digital Ground
15	MOSI/SDA/HW0	I	HiZ	Serial communication for SPI/I2C & HW0 interface pin, controlled by MODE
16	SCLK/SCL/HW1	I	HiZ	Serial Clock for SCLK (SPI), SCL (I2C), also HW1 controlled by MODE pin
17	MODE	I	HiZ	I2C/SPI Control selection or HW mode
18	MCLK	I	HiZ	Oscillator input
19	VCCA	Power	Power	Analog Supply, 3.3V
20	GPIO1	I/O	HiZ	General I/O w/extended functions
21	GPIO2	I/O	HiZ	General I/O w/extended functions
22	GPIO3	I/O	HiZ	General I/O w/extended functions
23	DGND	Ground	Ground	Digital Ground
24	DVDD	Power	Power	Digital Supply, 1.2V
25	DAC8	AO	Ground	Differential Positive Output for Channel 8
26	DAC8B	AO	Ground	Differential Negative Output for Channel 8
27	DAC6B	AO	Ground	Differential Negative Output for Channel 6
28	DAC6	AO	Ground	Differential Positive Output for Channel 6
29	AGND	Ground	Ground	DAC analog output stage ground
30	SS/ADDR1/HW2	I	HiZ	Serial communication for SPI/I2C & HW2 interface pin, controlled by MODE pin
31	MISO/ADDR0/ MUTE_CTRL	I	HiZ	Serial communication for SPI/I2C & MUTE_CTRL interface pin, controlled by MODE pin
32	AVCC_R	Power	Power	3.3V DAC analog output stage reference supply for the Right side
33	DAC4	AO	Ground	Differential Positive Output for Channel 4
34	DAC4B	AO	Ground	Differential Negative Output for Channel 4
35	DAC2B	AO	Ground	Differential Negative Output for Channel 2
36	DAC2	AO	Ground	Differential Positive Output for Channel 2
37	DVDD	Power	Power	Digital Supply, 1.2V
38	DGND	Ground	Ground	Digital Core Ground
39	DATA8/GPIO8	I/O	HiZ	Serial DATA8, General I/O 8
40	DATA7/GPIO7	I/O	HiZ	Serial DATA7, General I/O 7
41	DATA6/GPIO6	I/O	HiZ	Serial DATA6, General I/O 6
42	DATA5/GPIO5	I/O	HiZ	Serial DATA5, General I/O 5
43	DATA4/GPIO4	I/O	HiZ	Serial DATA4, General I/O 4
44	DATA3	I	HiZ	Serial DATA3 pin
45	DATA2	I	HiZ	Serial DATA2 pin
46	DATA1	I	HiZ	Serial DATA1 pin
47	DATA_CLK	I	HiZ	Serial Data Clock pin
48	AVDD	Power	Power	3.3V I/O Supply
49	External PAD	-	-	Only for ES9017Q, external pad, connect to AGND

\* Note: AO = Analog Output, I = Digital Input, I/O = Digital Input/Output



## Feature List

The ES9017 is a SABRE 8 channel high performance digital to analog converter (DAC) with features and performance including the new Hyperstream IV modulator that produces a device is well suited for a variety of applications.

In addition to improved performance, the new ES9017 SABRE DAC now supports the TDM audio interface, SPI (or I2C) control interface and hardware modes for simplifying device configuration.

TDM / I2S / LJ / RJ / DSD / DoP audio interfaces are supported.

Sample rates up to 768kHz (@ 64 FS) with PCM data and 7 selectable digital filters, and DSD rates up to DSD512 (512 x 44.1kHz) are supported.

## Configuration Modes

The ES9017 has 4 control programming modes. They are controlled by the state of the MODE (pin 17):

MODE PIN	Configuration
0	I <sup>2</sup> C interface
Pull Low	HW control mode (see Hardware Mode Table)
Pull High	HW control mode (see Hardware Mode Table)
1	SPI interface

Table 1 - Mode pin configuration options

## Software Mode

ES9017 supports I<sup>2</sup>C or SPI serial communication to configure registers. There are two types of registers, read/write and read-only registers.

### I<sup>2</sup>C

- MODE (Pin 17) – **GND**
- Connect per I<sup>2</sup>C standard
  - SDA (Pin 15)
  - SCL (Pin 16)
  - ADDR0 (Pin 31)
  - ADDR1 (Pin 30)

I <sup>2</sup> C Address	ADDR1	ADDR0
0x90	<b>GND</b>	<b>GND</b>
0x92	<b>GND</b>	<b>AVDD</b>
0x94	<b>AVDD</b>	<b>GND</b>
0x96	<b>AVDD</b>	<b>AVDD</b>

Table 2 – I<sup>2</sup>C addresses

### SPI

- Mode (Pin 17) – **AVDD**
- Connect per SPI standard
  - MOSI (Pin 15)
  - SCLK (Pin 16)
  - SS (Pin 30)
  - MISO (Pin 31)

SPI command	First byte
Write	<b>3</b>
Read	<b>1</b>

Table 3 - SPI commands

## Hardware Mode

The ES9017 has 19 pre-configured modes that can be set with external pin configuration. These modes configure the DAC for different input serial data rates and set the DAC muting.

These modes are set with pins:

- MODE (Pin 17)
- HW0 (Pin 15)
- HW1 (Pin 16)
- HW2 (Pin 30)
- MUTE\_CTRL (Pin 31)

Each hardware mode pin has 4 states:

- 0 – Pin directly connected to GND
- 1 – Pin directly connected to AVDD
- Pull 0 – Pin pulled to GND through 47kΩ resistor
- Pull 1 – Pin pulled to AVDD through 47kΩ resistor

## Design Information

Each hardware mode pin can be configured with either a pull-up or pull-down resistor. Therefore, it is important that the pin is configured to allow for the desired hardware modes. Some guidelines include the following:

- The HW0 and HW1 pins never require a pull up or pull-down resistor.

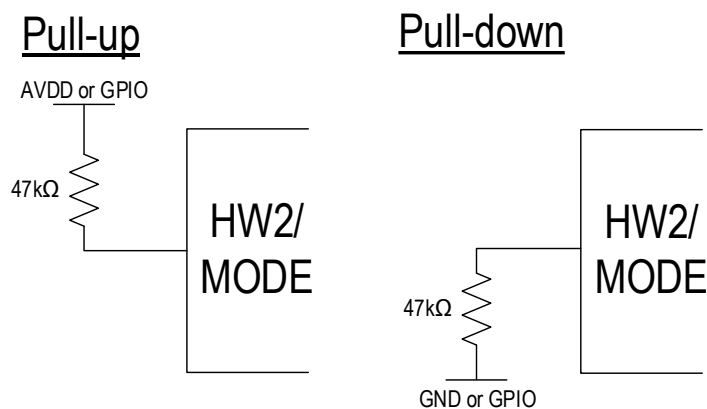


Figure 2 - Hardware mode pin configurations

## Muting

MUTE\_CTRL (Pin 31) is used to control the muting of the output and enabling of the Automute feature while in Hardware Mode:

- 0 – Output Muted, No Automute
- 1 – Output Unmuted, No Automute
- Pull 0 – Output Muted, Automute Enabled
- Pull 1 – Output Unmuted, Automute Enabled

## Hardware Mode Pin Configurations

The following table shows the available hardware modes for the ES9017. All modes require synchronous MCLK/FS/BCK or MCLK/DSDCLK.

HW #	Description	FS [kHz]	BCK [MHz]	MCLK [MHz]	MODE	HW2	HW1	HW0
0	I2S Master	MCLK/128	64*FS	128*FS	Pull 0	0	0	0
1	I2S Master	MCLK/256	64*FS	256*FS	Pull 0	0	0	1
2	I2S Master	MCLK/512	64*FS	512*FS	Pull 0	0	1	0
3	I2S Master	MCLK/1024	64*FS	1024*FS	Pull 0	0	1	1
4	LJ Master Mode	MCLK/128	64*FS	128*FS	Pull 0	Pull 0	0	0
5	LJ Master Mode	MCLK/256	64*FS	256*FS	Pull 0	Pull 0	0	1
6	LJ Master Mode	MCLK/512	64*FS	512*FS	Pull 0	Pull 0	1	0
7	LJ Master Mode	MCLK/1024	64*FS	1024*FS	Pull 0	Pull 0	1	1
8	I2S Slave SYNC, MCLK/1 (or DoP,DSD)	$8 \leq FS \leq 768$	64*FS	$64*FS \leq 1024*FS$ $2*DSDCLK \leq 16*DSDCLK$	Pull 0	Pull 1	0	0
9	I2S Slave SYNC, MCLK/2 (or DoP,DSD)	$8 \leq FS \leq 384$	64*FS	$128*FS \leq 1024*FS$ $4*DSDCLK \leq 45.1584$	Pull 0	Pull 1	0	1
10	I2S Slave SYNC, MCLK/4 (or DoP,DSD)	$8 \leq FS \leq 192$	64*FS	$256*FS \leq 1024*FS$ $8*DSDCLK \leq 45.1584$	Pull 0	Pull 1	1	0
11	I2S Slave SYNC, ACG (or DoP,DSD)	$8 \leq FS \leq 768$	64*FS	$64*FS \leq 1024*FS$ $2*DSDCLK \leq 45.1584$	Pull 0	Pull 1	1	1
12	LJ Slave SYNC, MCLK/1	$8 \leq FS \leq 768$	64*FS	$64*FS \leq 1024*FS$	Pull 0	1	0	0
13	LJ Slave SYNC, MCLK/2	$8 \leq FS \leq 384$	64*FS	$128*FS \leq 1024*FS$	Pull 0	1	0	1
14	LJ Slave SYNC, MCLK/4	$8 \leq FS \leq 192$	64*FS	$256*FS \leq 1024*FS$	Pull 0	1	1	0
15	LJ Slave SYNC, ACG	$8 \leq FS \leq 768$	64*FS	$64*FS \leq 1024*FS$	Pull 0	1	1	1
16	TDM LJ Slave SYNC, Autodetect CH num	$8 \leq FS \leq 192$	Auto (256FS/512FS/1024FS)	$256*FS \leq 49.152$	Pull 1	1	0	0
17	TDM LJ Slave SYNC, Autodetect CH num	$8 \leq FS \leq 96$	Auto (512FS/1024FS)	$512*FS \leq 49.152$	Pull 1	1	0	1
18	TDM LJ Slave SYNC, Autodetect CH num	$8 \leq FS \leq 48$	Auto (1024FS)	$1024*FS \leq 49.152$	Pull 1	1	1	0
19	TDM LJ Slave SYNC, Autodetect CH num	$8 \leq FS \leq 48$	Auto (1024FS)	$1024*FS \leq 49.152$	Pull 1	1	1	1

Table 4 - Hardware mode pin configurations table

**Note:**

\*ACG is auto clock gearing is enabled, it will normally gear the clock down to 128\*FS, unless 64\*FS is required, or 2\*DSDCLK in DSD modes.

**\*To enable DoP/DSD in HW mode, DATA8/GPIO8 pin must be high**

\*Mode 16 = Channel Slots 1 to 8, Mode 17 = Channel Slots 9 to 16, Mode 18 = Channel slots 17 to 24, Mode 19 = Channel slots 25 to 32.



### Recommended Hardware Mode Setup Sequence

The hardware mode setup sequence is shown below with all hardware pins being defined after CHIP\_EN is asserted.

*Note: It is recommended that MUTE\_CTRL is set low until the HW mode is finalized and after CHIP\_EN is asserted, then asserted last.*

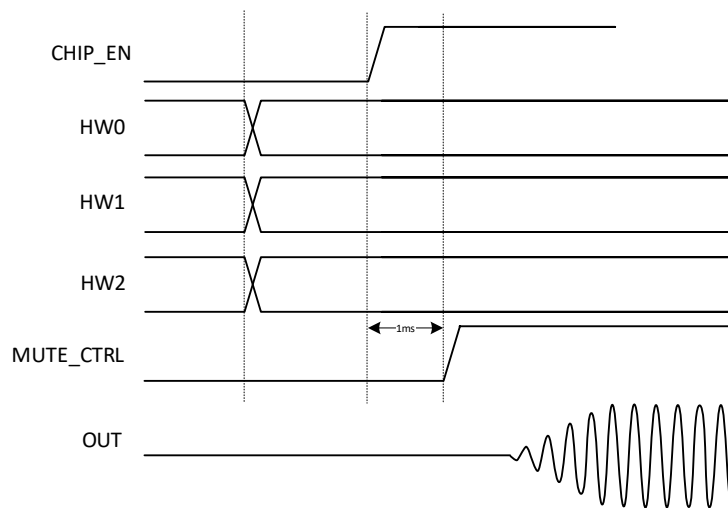
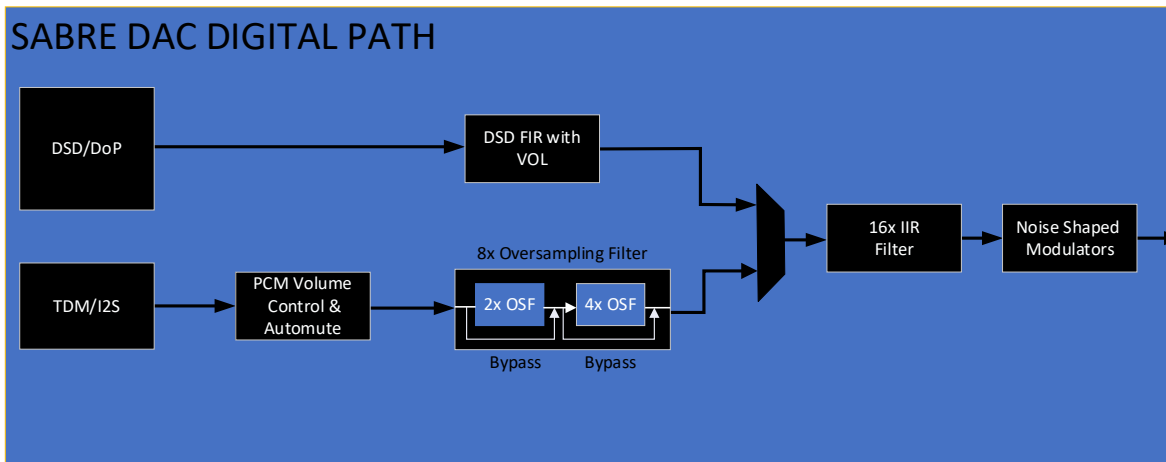


Figure 3 - Hardware mode startup sequence

## Digital Features

See Recommended Operating Conditions for additional information.

### Digital Signal Path



### GPIO Configuration

GPIO_CONFIG	Function	I/O Direction
0	Analog Shutdown*	N/A
1	1'b0	Output
2	1'b1	Output
3	CLK_IDAC output	Output
4	Reserved	N/A
5	Mute all channel	Input
6	Input Selection	Input
7	Lock status	Output
8	CLK_VALID	Output
9	TDM_VALID	Output
10	DOP_VALID	Output
11	BCK_WS_FAIL	Output
12	Volume min	Output
13	Automute status	Output
14	Soft Ramp finished	Output
15	Reserved	N/A

Table 5 - GPIO Configuration functions

Note: DoP Valid is for channel 1 & 2, as a channel pair

For GPIO\_CONFIG 0:

\*Analog Shutdown is input disabled, output is tri-stated

GPIOx Default states:

GPIO1: Automute Status (GPIO\_CONFIG = 13)

GPIO2-8: Analog Shutdown (GPIO\_CONFIG = 0)



## Audio Input Formats

### PCM (subset of TDM interface)

Data is organized as 2 channels per data line. Any channel on any data line can be mapped to any DAC through the TDM\_CHx\_CONFIG channel mapping Registers 32-39. Data is latched on the positive edge of BCLK.

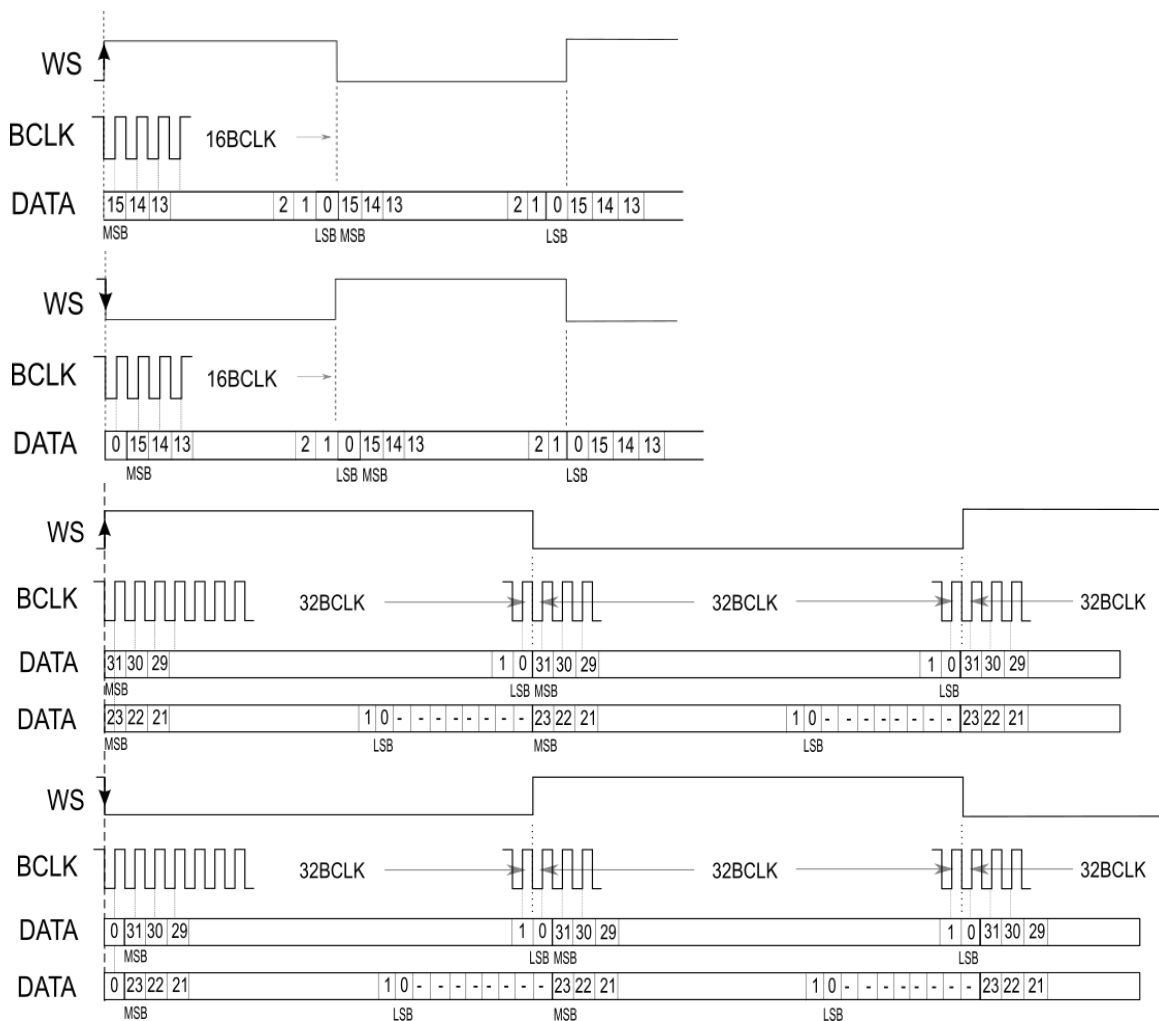


Figure 4 – LJ & I2S Input for 16bit and 32bit word depths

Note: RJ is supported but only in software mode.



**Time-division multiplexing (TDM)**

The ES9017 supports time-division multiplexing (TDM) format, allowing more than 2 channels (or slots) to be transmitted on each data line, up to a maximum of 32 channels per data line. Typical formats are TDM128 (4chx32bit), TDM256 (8chx32bit), TDM512 (16chx32bit) and TDM1024 (32chx32bit). In this mode, the TDM\_CHx\_CONFIG channel mapping Registers 32-39 can be used to internally map any slot (channel) to any DAC. Data is latched on the positive edge of BCLK.

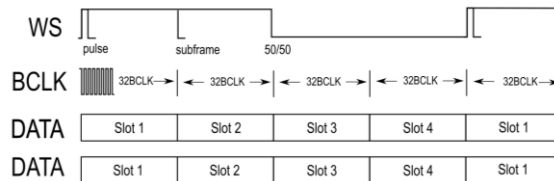


Figure 5 – TDM128 mode

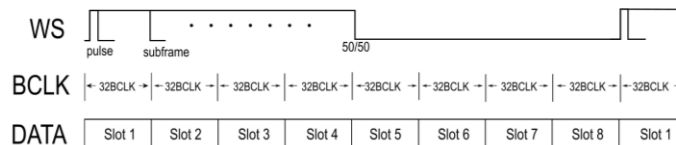


Figure 6 – TDM256 mode

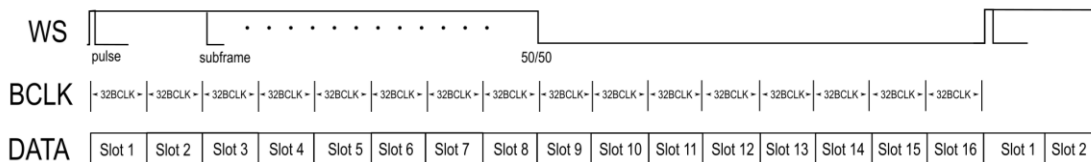


Figure 7 – TDM512 mode

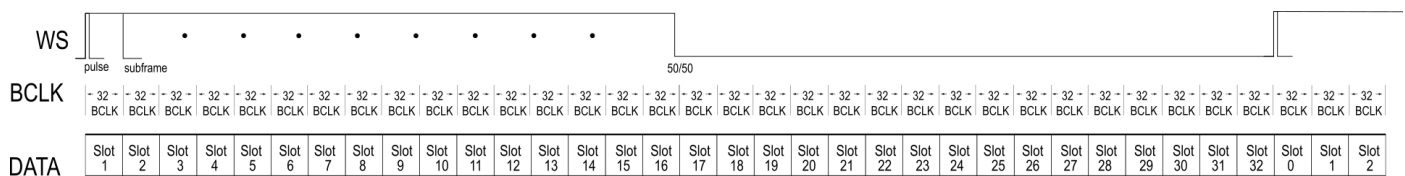


Figure 8 – TDM1024 mode



**DSD<sup>1</sup>**

In DSD mode, there is a single DSD clock line, and each channel of data is an additional DSD data line. There is no internal channel mapping for DSD input, DSD data input to DATA1 is sent to Ch1, DSD data input to DATA2 is sent to Ch2, etc.

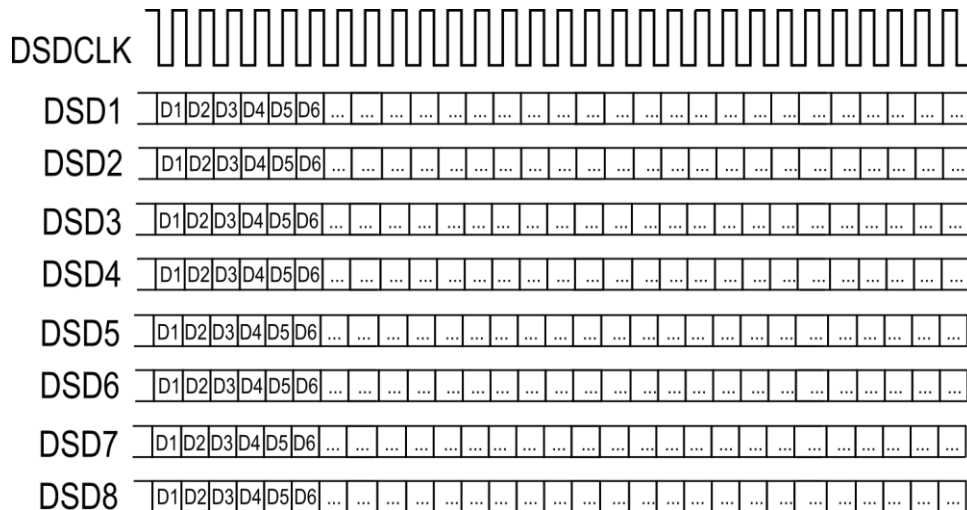


Figure 9 – DSD format, 1bit stream

<sup>1</sup> The Automute Feature is not available when using DSD mode



## Pre-Programmed Digital Filters

The ES9017 has 7 pre-programmed digital filters. The latency for each filter reduces (scales) with increasing sample rates. (See Register 88[2:0] for configuration). The filters are:

- Minimum Phase (default)
- Linear Phase Apodizing
- Linear Phase Fast Roll-off
- Linear Phase Slow Roll-off
- Minimum Phase Fast Roll-off
- Minimum Phase Slow Roll-off
- Minimum Phase Slow Roll-off Low Dispersion

### PCM Filter Properties (48kHz Sampling)

Minimum Phase					
Parameter	Conditions	MIN	TYP	MAX	UNIT
Pass band	-3dB			0.49 x fs	Hz
Stop band	-97dB	0.55 x fs			Hz
Group Delay		3.29/fs		9.37/fs	s
Flatness (ripple)	0.0004				dB

Linear Phase Apodizing					
Parameter	Conditions	MIN	TYP	MAX	UNIT
Pass band	-3dB			0.44 x fs	Hz
Stop band	-107dB	0.5 x fs			Hz
Group Delay			33.2/fs		s
Flatness (ripple)	0.0017				dB

Linear Phase Fast Roll-off					
Parameter	Conditions	MIN	TYP	MAX	UNIT
Pass band	-3dB			0.49 x fs	Hz
Stop band	-118dB	0.55 x fs			Hz
Group Delay			33.8/fs		s
Flatness (ripple)	0.0023				dB

Linear Phase Slow Roll-off					
Parameter	Conditions	MIN	TYP	MAX	UNIT
Pass band	-3dB			0.44 x fs	Hz
Stop band	-84dB	0.74 x fs			Hz
Group Delay			5.62/fs		s
Flatness (ripple)	0.002				dB



Minimum Phase Fast Roll-off					
Parameter	Conditions	MIN	TYP	MAX	UNIT
Pass band	-3dB			0.48 x fs	Hz
Stop band	-99dB	0.55 x fs			Hz
Group Delay		3.29/fs		9.51/fs	s
Flatness (ripple)	0.0016				dB

Minimum Phase Slow Roll-off					
Parameter	Conditions	MIN	TYP	MAX	UNIT
Pass band	-3dB			0.43 x fs	Hz
Stop band	-84dB	0.79 x fs			Hz
Group Delay		2.5/fs		3/fs	s
Flatness (ripple)	0.0035				dB

Minimum Phase Slow Roll-off Low Dispersion					
Parameter	Conditions	MIN	TYP	MAX	UNIT
Pass band	-3dB			0.43 x fs	Hz
Stop band	-84dB	0.79 x fs			Hz
Group Delay		9.7/fs		9.9/fs	s
Flatness (ripple)	0.0053				dB

Table 6 – PCM Filter Properties

### PCM Filter Latency

The following table shows the simulated latency of each filter at 48kHz sampling rate. Latency delay will reduce (scale) with sampling rate.

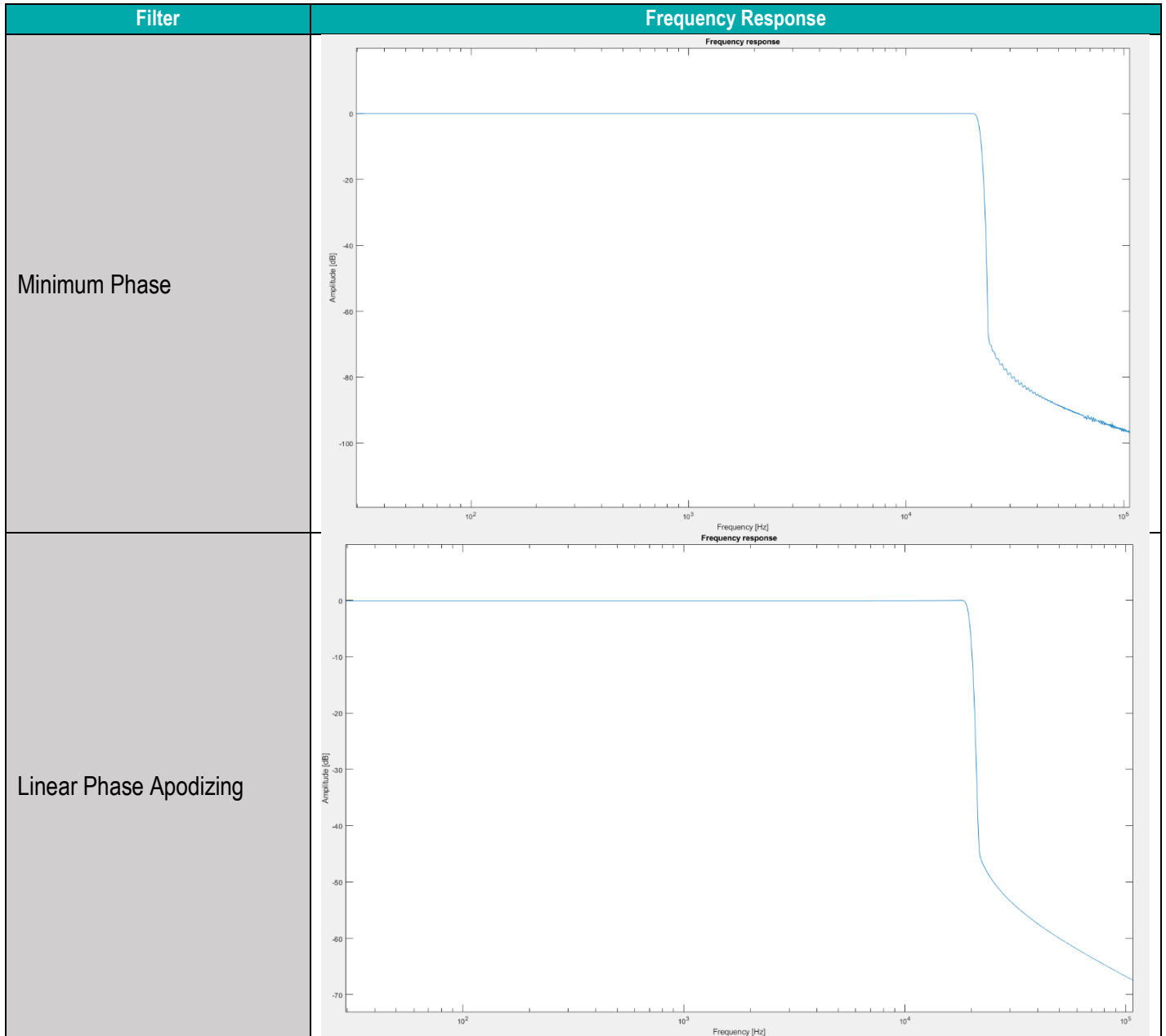
Digital Filter	Delay(us) @ fs=48kHz
Minimum phase (default)	158us
Linear Phase Apodizing	760us
Linear Phase Fast Roll-Off	771us
Linear Phase Slow Roll-Off	208us
Minimum Phase fast roll-off	158us
Minimum Phase slow roll-off	137us
Minimum Phase Slow roll-off low dispersion	282us

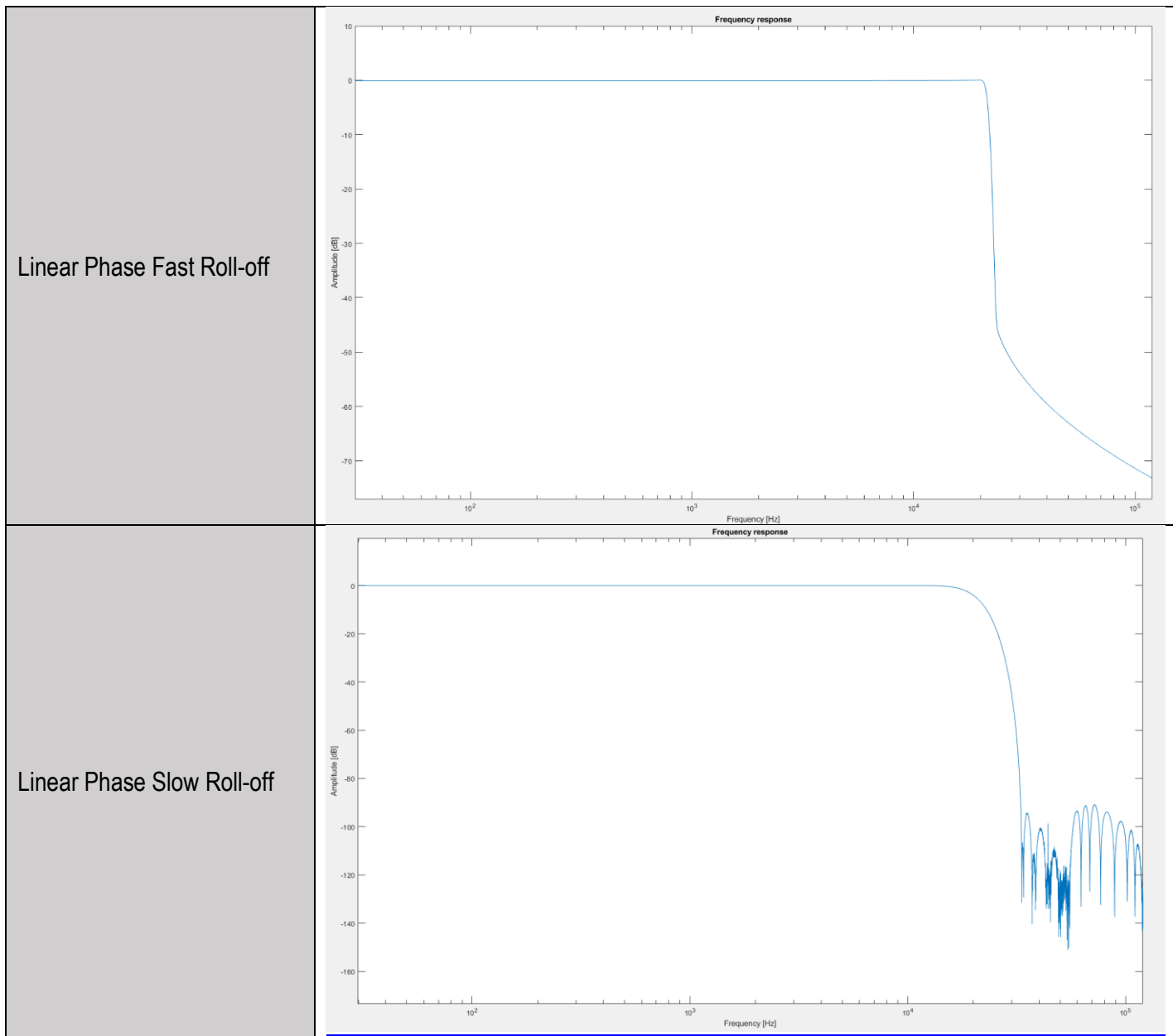
Table 7 - Latency of Pre-Programmed Digital Filters

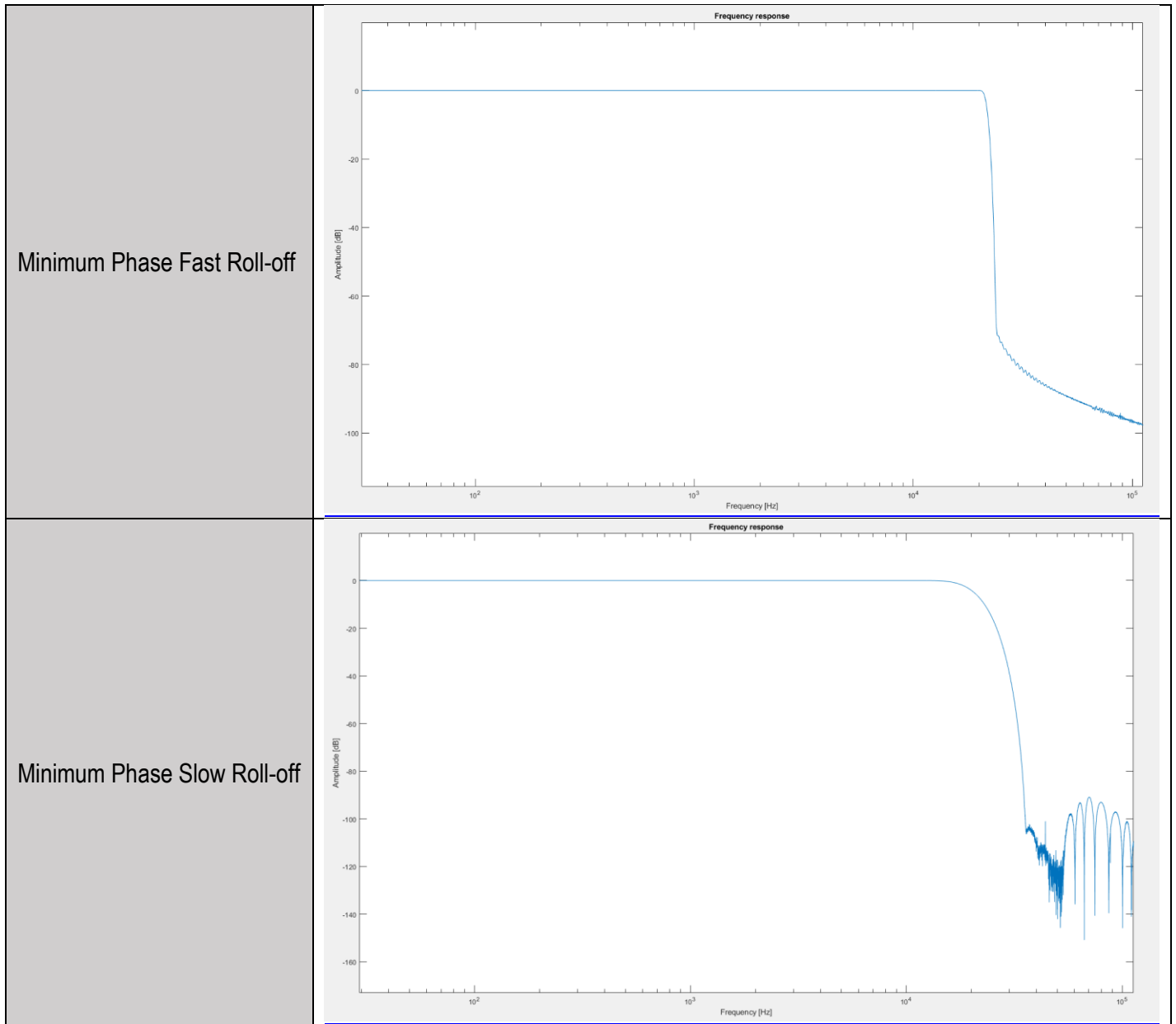


**PCM Filter Frequency Response**

The following frequency responses were obtained from software simulations of these filters. Simulation sample rate is 44.1kHz.







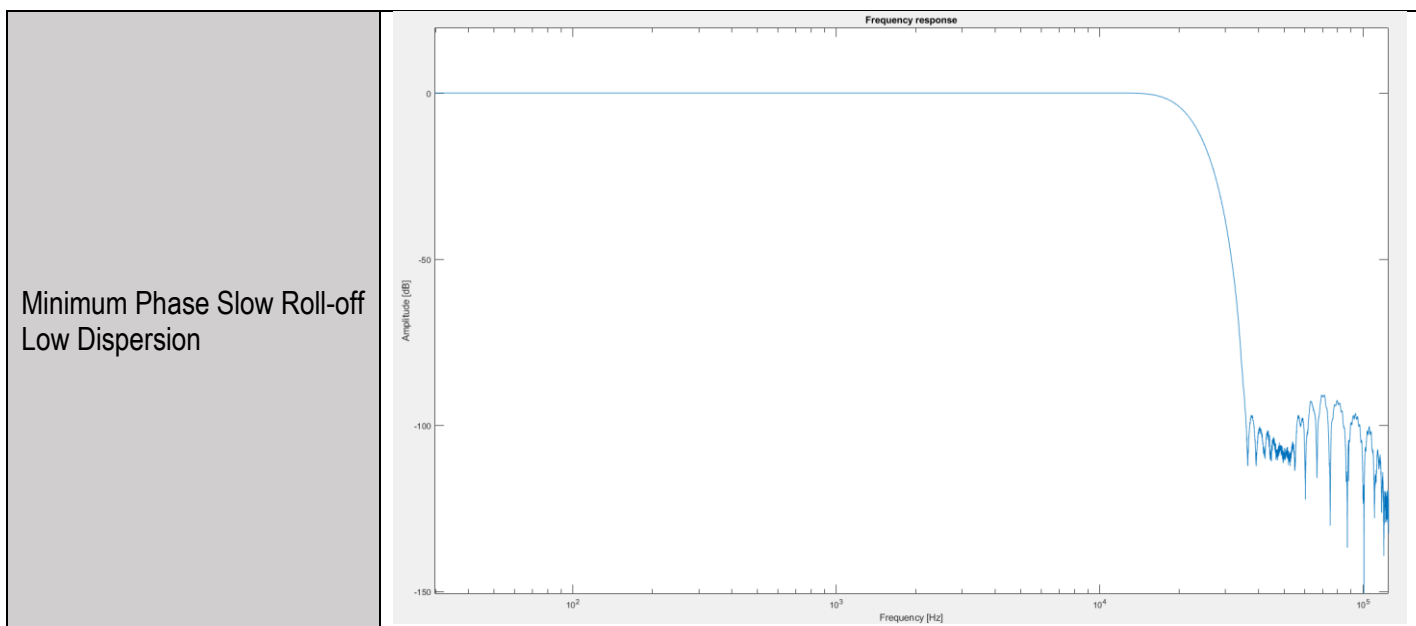
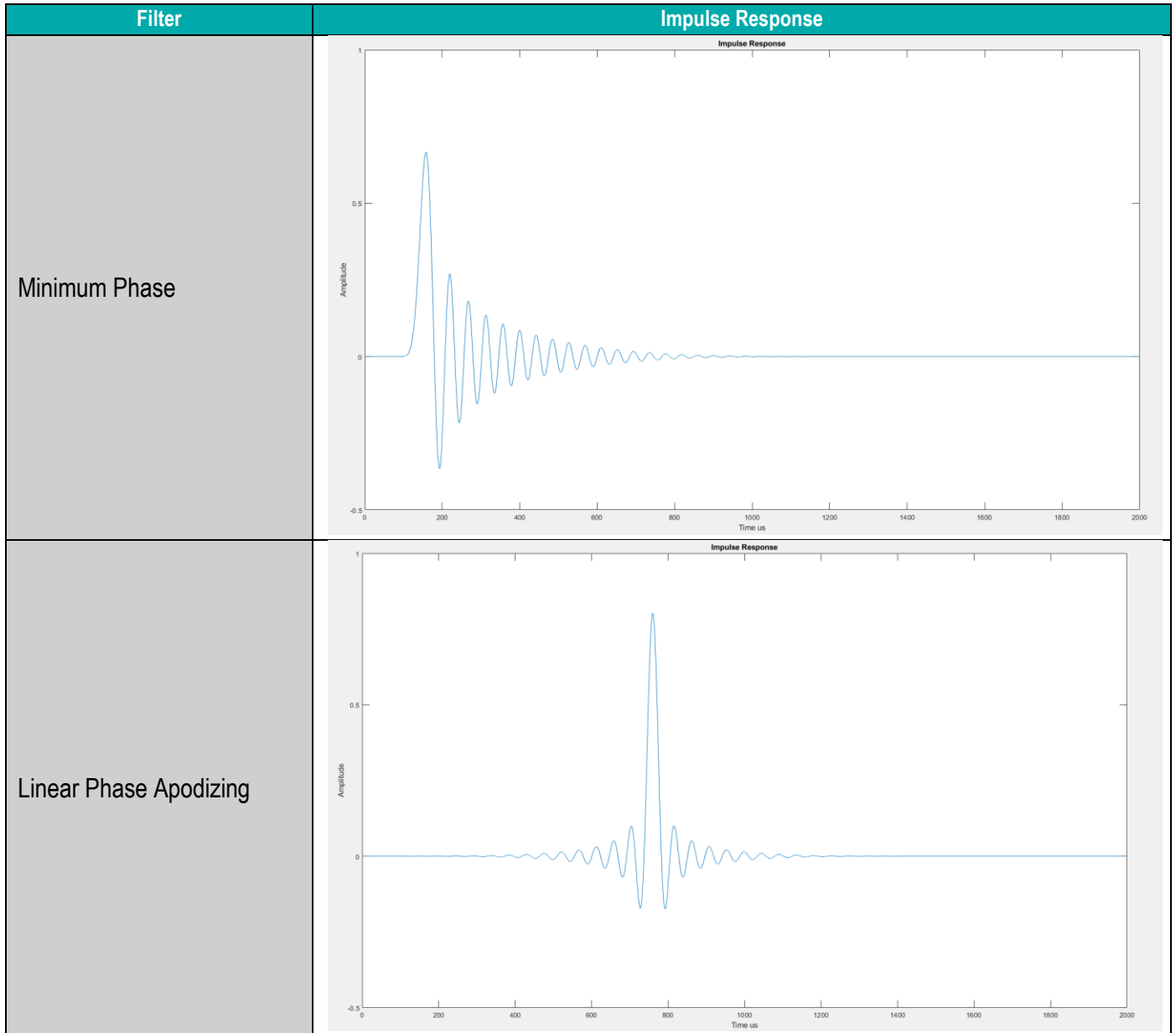


Table 8 – PCM Filter Frequency Response

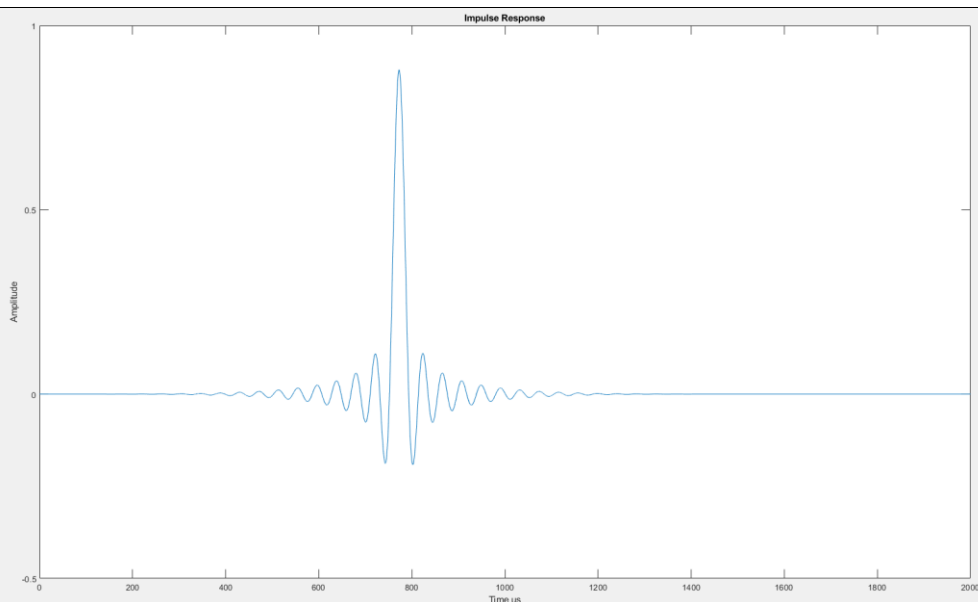
**PCM Filter Impulse Response**

The following impulse responses were obtained from software simulations of these filters. Simulation sample rate is 44.1kHz.

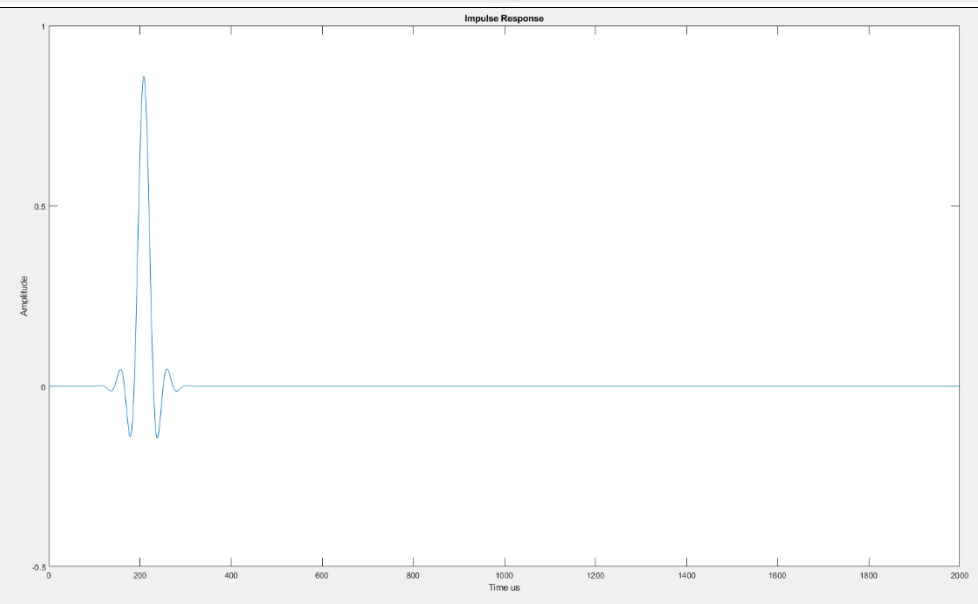




Linear Phase Fast Roll-off

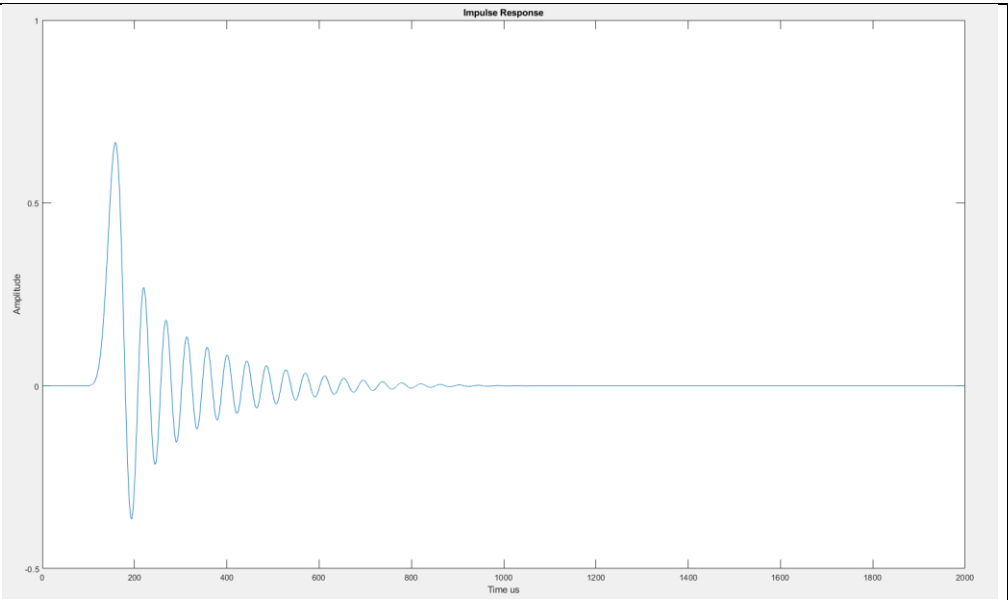


Linear Phase slow roll-off

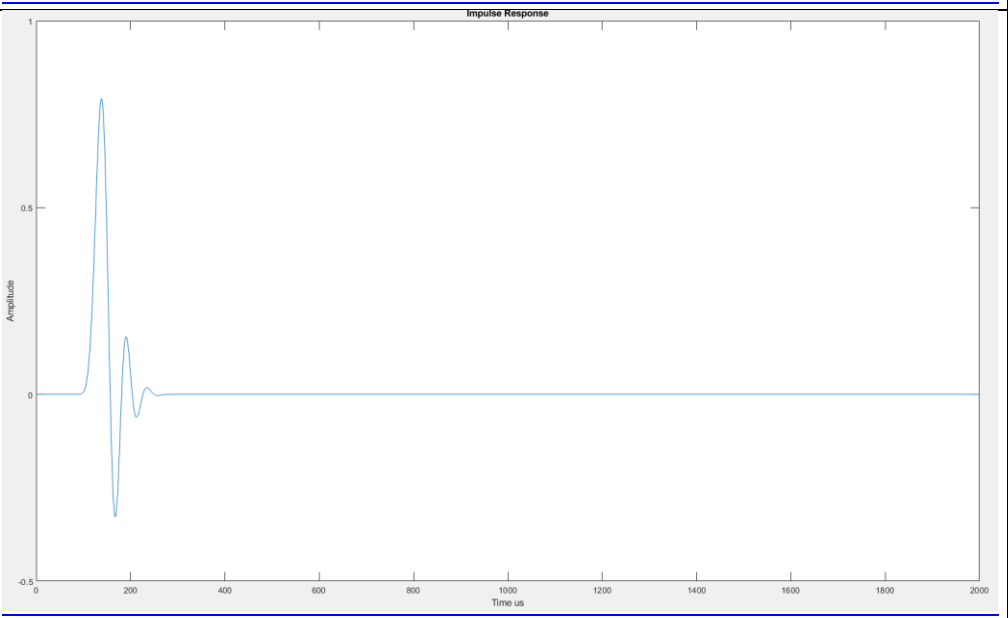




Minimum phase fast roll-off



Minimum phase slow roll-off





Minimum phase slow roll-off  
low dispersion

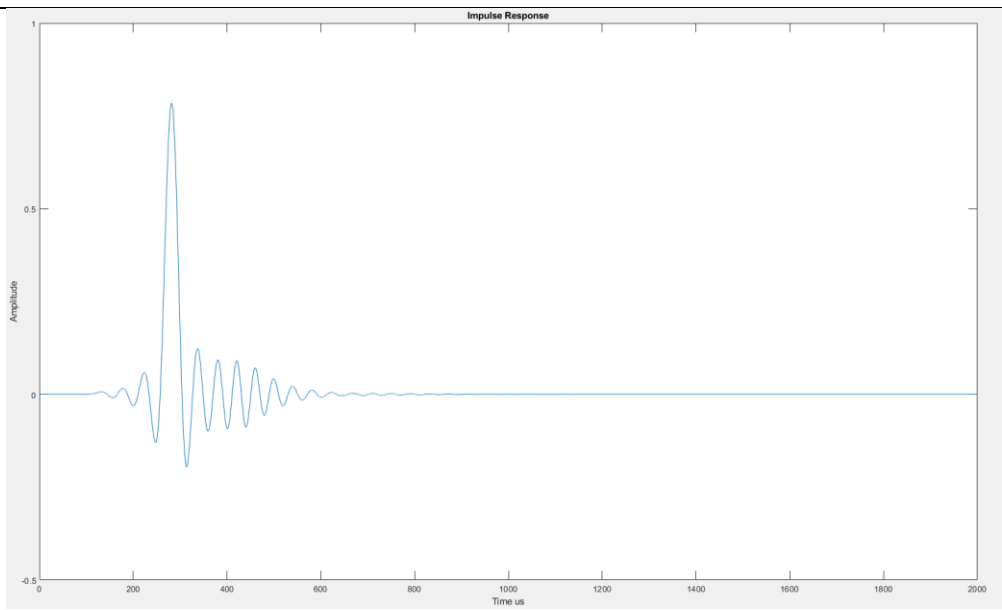


Table 9 – PCM Filter Impulse Response

## Absolute Maximum Ratings

PARAMETER	RATING
Positive Supply Voltage <ul style="list-style-type: none"> <li>• AVCC_L</li> <li>• AVCC_R</li> <li>• AVDD</li> <li>• VCCA</li> <li>• DVDD</li> </ul>	<ul style="list-style-type: none"> <li>• +3.7V with respect to Ground</li> <li>• +3.7V with respect to Ground</li> <li>• +3.7V with respect to Ground</li> <li>• +3.7V with respect to Ground</li> <li>• +1.4V with respect to Ground</li> </ul>
Storage temperature	-65°C to +150°C
Operating Junction Temperature	+125°C
Voltage range for digital input pins	-0.3V to AVDD(nom)+0.3V
ESD Protection	
Human Body Model (HBM)	2kV
Charge Device Model (CDM)	500V

Table 10 – Absolute Maximum Ratings

**WARNING:** Stresses beyond those listed under here may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied.

**WARNING:** Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

## I/O Electrical Characteristics

PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNIT	COMMENTS
High-level input voltage	VIH	$(AVDD / 2) + 0.4$		V	
Low-level input voltage	VIL		0.4	V	
High-level output voltage	VOH	$AVDD - 0.2$		V	
Low-level output voltage	VOL		0.2	V	

Table 11 – I/O Electrical Characteristics



## Recommended Operating Conditions

There are the recommended operating conditions for the ES9017

PARAMETER	SYMBOL	CONDITIONS
Operating temperature	T <sub>A</sub>	-20°C to +85°C
AVCC_L		3.3V
AVCC_R		3.3V
AVDD		3.3V
VCCA		3.3V
DVDD		1.2V

Table 12 – Recommended Operating Conditions

## Clock Requirements

In slave mode, the ES9017 Sabre DAC requires synchronization between incoming serial audio FS/BCK clocks and the main external clock MCLK.

For example, if using a 49.152MHz MCLK is used, sample rate would be multiples of 48kHz (ie. 96kHz, 192kHz, 384kHz).

When using the highest PCM sample rates (705.6kHz & 768kHz), Register 0[6] ENABLE\_64FS\_MODE is required to use the DAC in 64FS mode.

Sampling Rate	Multiplier	MCLK (MHz)
44.1kHz	1x	5.6448 (128FS)
	2x	11.2896 (256FS)
	4x	22.5792 (512FS)
	8x	45.1584 (1024FS)
48kHz	1x	6.144MHz (128FS)
	2x	12.288 (256FS)
	4x	24.576 (512FS)
	8x	49.152 (1024FS)

Table 13 – MCLK vs Sampling rates multipliers

\*For best performance, a higher MCLK/FS ratio is recommended, see the EVB manual for more details.

## Power Consumption

Power numbers are given when the device is in slave mode.

Test Conditions 1 (unless otherwise noted)

T<sub>A</sub> = 25°C, AVCC\_R = AVCC\_L = VCCA = AVDD = +3.3V, DVDD = +1.2V, fs = 48kHz, DAC enabled, 1kHz sine full scale

Parameter	Min	Typ	Max	Unit
<b>Hardware Mode: 11 (Slave mode with ACG (128*FS), MCLK = 49.152MHz)</b>				
AVCC_R		6.55		mA
AVCC_L		6.55		mA
VCCA		0.34		mA
AVDD		0.12		mA
DVDD		7.26		mA
<b>Power Consumption</b>		<b>53.4</b>		<b>mW</b>
<b>Hardware Mode: 2 (Master mode with MCLK = 24.576MHz, FS=MCLK/512)</b>				
AVCC_R		8.4		mA
AVCC_L		8.4		mA
VCCA		0.46		mA
AVDD		2.3		mA
DVDD		10.8		mA
<b>Power Consumption</b>		<b>77.4</b>		<b>mW</b>
<b>Hardware Mode: 1 (Master mode with MCLK = 12.288MHz, FS=MCLK/256)</b>				
AVCC_R		7.1		mA
AVCC_L		7.1		mA
VCCA		0.23		mA
AVDD		2.3		mA
DVDD		8.4		mA
<b>Power Consumption</b>		<b>65.8</b>		<b>mW</b>

Table 14 – Power Consumption with test conditions 1



Test Conditions 2 (unless otherwise noted)

T<sub>A</sub> = 25°C, AVCC\_R = AVCC\_L = VCCA = AVDD = +3.3V, DVDD = +1.2V, fs = 48kHz, DAC enabled, streaming zeros, automute enabled

Parameter	Min	Typ	Max	Unit
<b>Hardware Mode: 11 (Slave mode with ACG (128*FS), MCLK = 49.152MHz)</b>				
AVCC_R		0.6		mA
AVCC_L		0.6		mA
VCCA		0.34		mA
AVDD		0.19		mA
DVDD		2.6		mA
<b>Power Consumption</b>		<b>8.7</b>		<b>mW</b>
<b>Hardware Mode: 2 (MCLK = 24.576MHz)</b>				
AVCC_R		2.25		mA
AVCC_L		2.25		mA
VCCA		0.46		mA
AVDD		2.4		mA
DVDD		5.2		mA
<b>Power Consumption</b>		<b>30.3</b>		<b>mW</b>
<b>Hardware Mode: 1 (MCLK = 12.288MHz)</b>				
AVCC_R		1.1		mA
AVCC_L		1.1		mA
VCCA		0.3		mA
AVDD		2.4		mA
DVDD		3.5		mA
<b>Power Consumption</b>		<b>20.1</b>		<b>mW</b>

Table 15 – Power Consumption with test conditions 2

## Performance

Test Conditions 1 (unless otherwise noted)

$T_A = 25^\circ\text{C}$ ,  $AVCC\_R = AVCC\_L = VCCA = AVDD = +3.3\text{V}$ ,  $DVDD = +1.2\text{V}$ ,  $f_s = 48\text{kHz}$ , HW mode (I2S Master Mode)

Note: Performance numbers were measured using the ESS ES9017 evaluation board v1.1

Parameter		Min	Typ	Max	Unit
Resolution			32		Bit
Max MCLK frequency				50	MHz
THD+N Ratio / THD Ratio @ $f_s=48\text{kHz}$ (differential)	0dBFS, BW=20Hz-20kHz		-110		dB
THD+N Ratio / THD Ratio @ $f_s=96\text{kHz}$ (differential)	0dBFS, BW=20Hz-40kHz		-108		dB
THD+N Ratio / THD Ratio @ $f_s=192\text{kHz}$ (differential)	0dBFS, BW=20Hz-80kHz		-106		dB
THD+N Ratio / THD Ratio @ $f_s=384\text{kHz}$ (differential)	0dBFS, BW=20Hz-160kHz		-104		dB
DNR (A-weighted) (8 Channel mode – Single Channel diff)	-60dBFS		120		dB
DNR (A-weighted) (Stereo mode – 4 channel sum diff)			124		dB
DNR (A-weighted) (Mono mode – 8 channel sum diff)			126		dB
Voltage output amplitude	Full-scale out		$0.879 \times AVCC$		V <sub>pp</sub>
Voltage output offset	Bipolar zero out		$AVCC/2$		V
Current output amplitude	Full-scale out		$1000 \times 0.879 \times AVCC / R_{dac}$		mApp
Current output offsets	Bipolar zero out		$1000 \times (AVCC/2 - V_g) / R_{dac}$		mA
Output impedance (Per + or – pin of each differential DAC output pair)	$R_{DAC}$		$1563 \pm 15\%$		$\Omega$

Table 16 – Performance Data

## Timing Requirements

### I<sup>2</sup>C Slave Interface Timing

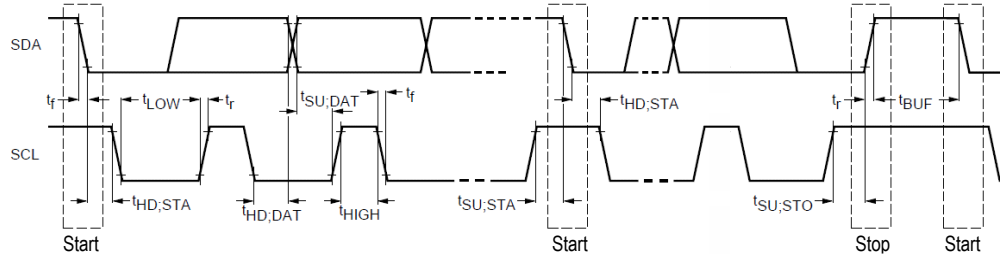


Figure 10 – I<sup>2</sup>C Slave Control Interface Timing

Parameter	Symbol	CLK Constraint	Standard-Mode		Fast-Mode		Unit
			MIN	MAX	MIN	MAX	
SCL Clock Frequency	$f_{SCL}$	$< CLK/20$	0	100	0	400	kHz
START condition hold time	$t_{HD,STA}$		4.0	-	0.6	-	$\mu s$
LOW period of SCL	$t_{LOW}$	$>10/CLK$	4.7	-	1.3	-	$\mu s$
HIGH period of SCL ( $>10/CLK$ )	$t_{HIGH}$	$>10/CLK$	4.0	-	0.6	-	$\mu s$
START condition setup time (repeat)	$t_{SU,STA}$		4.7	-	0.6	-	$\mu s$
SDA hold time from SCL falling - All except NACK read - NACK read only	$t_{HD,DAT}$		0 2/CLK	-	0 2/CLK	-	$\mu s$ s
SDA setup time from SCL rising	$t_{SU,DAT}$		250	-	100	-	ns
Rise time of SDA and SCL	$t_r$		-	1000		300	ns
Fall time of SDA and SCL	$t_f$		-	300		300	ns
STOP condition setup time	$t_{SU,STO}$		4	-	0.6	-	$\mu s$
Bus free time between transmissions	$t_{BUF}$		4.7	-	1.3	-	$\mu s$
Capacitive load for each bus line	$C_b$		-	400	-	400	pF

Table 17 – I<sup>2</sup>C slave/synchronous slave interface timing definitions

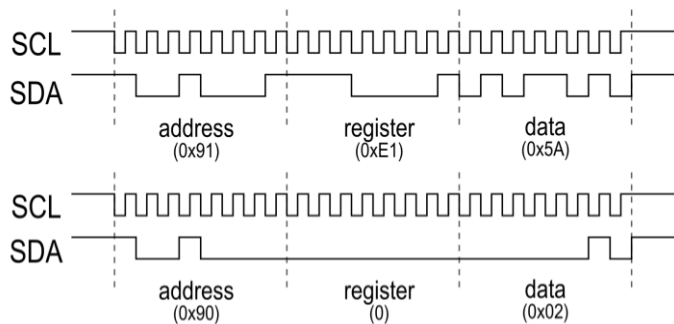


Figure 11 – I<sup>2</sup>C single byte examples of read and write instructions with I<sup>2</sup>C



## SPI Slave Interface

The 4-wire SPI data format is: Command (1 byte) + Address (1 byte) + Data

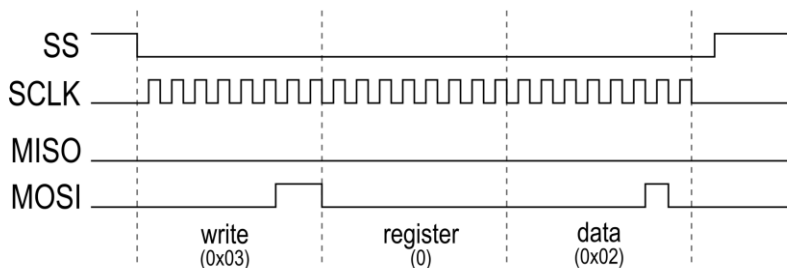


Figure 12 – SPI single byte write

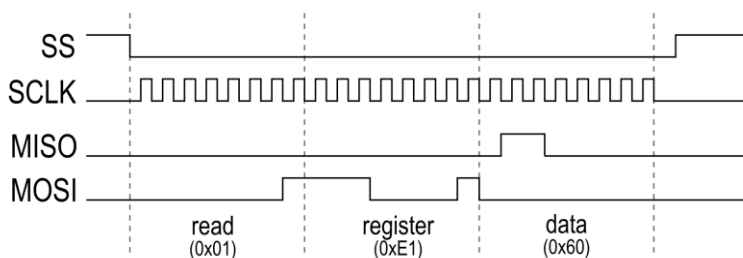


Figure 13 – SPI single byte read

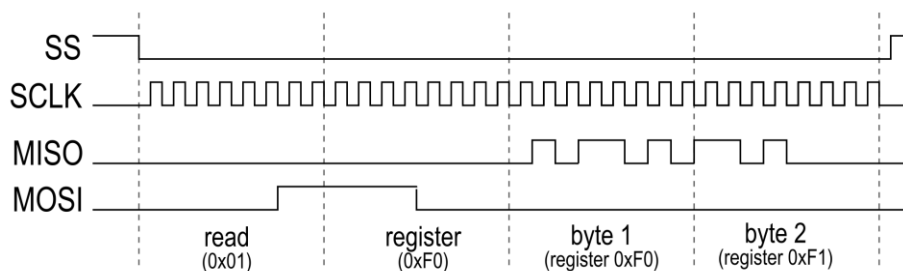


Figure 14 – SPI multi-byte read



## Register Overview

The ES9017 contains read/write and read-only registers. A system clock must be present to access registers.

Multi-byte registers must be written from LSB to MSB. Data is latched when MSB is written.

Multi-byte registers must be read from LSB to MSB. Data is latched when LSB is read.

MSB is always stored in the highest register address.

### **Read/Write Register Addresses**

Registers 0-65 (0x00 – 0x41) are read/write registers

### **Read-only Register Addresses**

Registers 224 – 233 (0xE0 – 0xE9) are read only registers.

### **Multi-Byte Registers**

Multi-byte registers must be written from LSB to MSB. Data is latched when MSB is written.

MSB is always stored in the highest register address.



# Register Map

Addr (Hex)	Addr (Dec)	Register	7	6	5	4	3	2	1	0	
0x00	0	SYSTEM CONFIG	SOFT_RESET	ENABLE_64FS_MODE	RESERVED	ENABLE_DOP_DECODE	ENABLE_DSD_DECODE	ENABLE_TDM_DECODE	DAC_MODE_REG	RESERVED	
0x01	1	SYS MODE CONFIG	RESERVED		ENABLE_DAC_CLK	ENABLE_NSMD_CLK	RESERVED				
0x02	2	DAC CLOCK CONFIG	AUTO_FS_DETECT	SELECT_IDAC_HALF	SELECT_IDAC_NUM						
0x03	3	CLOCK CONFIG	MASTER_BCK_DIV								
0x04	4	CONFIG	RESERVED		SEL_CLK		RESERVED	AUTO_CLK_GE_AR	RESERVED		
0x05 - 0x0F	5 - 15	RESERVED	RESERVED								
0x10	16	GPIO1/2 CONFIG	GPIO2_CFG				GPIO1_CFG				
0x11	17	GPIO3/4 CONFIG	GPIO4_CFG				GPIO3_CFG				
0x12	18	GPIO5/6 CONFIG	GPIO6_CFG				GPIO5_CFG				
0x13	19	GPIO7/8 CONFIG	GPIO8_CFG				GPIO7_CFG				
0x14	20	GPIO OUTPUT ENABLE	GPIO8_OE	GPIO7_OE	GPIO6_OE	GPIO5_OE	GPIO4_OE	GPIO3_OE	GPIO2_OE	GPIO1_OE	
0x15	21	GPIO INPUT	GPIO8_SDB	GPIO7_SDB	GPIO6_SDB	GPIO5_SDB	GPIO4_SDB	GPIO3_SDB	GPIO2_SDB	GPIO1_SDB	
0x16	22	RESERVED	RESERVED								
0x17	23	GPIO OUTPUT LOGIC	GPIO_SEL		GPIO_OR_SS_RAMP	GPIO_OR_VOL_MIN	GPIO_OR_AUTOMUTE	GPIO_AND_SS_RAMP	GPIO_AND_VOL_MIN	GPIO_AND_AUTOMUTE	
0x18	24	GPIO OUTPUT LOGIC	GPIO_DAC_MODE	RESERVED						GPIO_SEL	
0x19	25	INPUT SELECTION	AUTO_CH_DETECT	ENABLE_DSD_FAULT_DETECTION	DSD_MASTER_MODE	PCM_MASTER_MODE	RESERVED	INPUT_SEL		AUTO_INPUT_SEL	
0x1A	26	SERIAL MASTER ENCODER CONFIG	TDM_RESYNC	BCK_INV	RESERVED	MASTER_FRAME_LENGTH		MASTER_WS_PULSE_MODE	MASTER_WS_INVERT	MASTER_BCK_INVERT	
0x1B	27	TDM CONFIG	RESERVED			TDM_CH_NUM					
0x1C	28	TDM CONFIG1	TDM_LJ_MODE	TDM_VALID_EDGE	RESERVED						
0x1D	29	TDM CONFIG2	RESERVED	TDM_BIT_WIDTH		TDM_DATA_LATCH_ADJ					
0x1E	30	BCK/WS MONITOR CONFIG	DISABLE_DSD_DC	DISABLE_DSD_MUTE	ENABLE_WS_MONITOR	ENABLE_BCK_MONITOR	DISABLE_PCM_DC	RESERVED			
0x1F	31	RESERVED	RESERVED								
0x20	32	TDM CH1 CONFIG	RESERVED	TDM_CH1_LINE_SEL			TDM_CH1_SLOT_SEL				
0x21	33	TDM CH2 CONFIG	RESERVED	TDM_CH2_LINE_SEL			TDM_CH2_SLOT_SEL				
0x22	34	TDM CH3 CONFIG	RESERVED	TDM_CH3_LINE_SEL			TDM_CH3_SLOT_SEL				
0x23	35	TDM CH4 CONFIG	RESERVED	TDM_CH4_LINE_SEL			TDM_CH4_SLOT_SEL				
0x24	36	TDM CH5 CONFIG	RESERVED	TDM_CH5_LINE_SEL			TDM_CH5_SLOT_SEL				
0x25	37	TDM CH6 CONFIG	RESERVED	TDM_CH6_LINE_SEL			TDM_CH6_SLOT_SEL				
0x26	38	TDM CH7 CONFIG	RESERVED	TDM_CH7_LINE_SEL			TDM_CH7_SLOT_SEL				
0x27	39	TDM CH8 CONFIG	RESERVED	TDM_CH8_LINE_SEL			TDM_CH8_SLOT_SEL				
0x28	40	VOLUME1	VOLUME1								
0x29	41	VOLUME2	VOLUME2								
0x2A	42	VOLUME3	VOLUME3								
0x2B	43	VOLUME4	VOLUME4								
0x2C	44	VOLUME5	VOLUME5								
0x2D	45	VOLUME6	VOLUME6								
0x2E	46	VOLUME7	VOLUME7								
0x2F	47	VOLUME8	VOLUME8								
0x30	48	DAC VOL UP RATE	DAC_VOL_RATE_UP								
0x31	49	DAC VOL DOWN RATE	DAC_VOL_RATE_DOWN								
0x32	50	DAC VOL DOWN RATE FAST	DAC_VOL_RATE_FAST								
0x33	51	DAC MUTE	DAC_MUTE_CH8	DAC_MUTE_CH7	DAC_MUTE_CH6	DAC_MUTE_CH5	DAC_MUTE_CH4	DAC_MUTE_CH3	DAC_MUTE_CH2	DAC_MUTE_CH1	
0x34	52	DAC INVERT	DAC_INVERT_CH8	DAC_INVERT_CH7	DAC_INVERT_CH6	DAC_INVERT_CH5	DAC_INVERT_CH4	DAC_INVERT_CH3	DAC_INVERT_CH2	DAC_INVERT_CH1	
0x35	53	FILTER SHAPE	RESERVED						FILTER SHAPE		
0x36	54	IIR BANDWIDTH	RESERVED						VOLUME_HOLD	IIR_BW	
0x37	55	DAC PATH CONFIG	RESERVED						BYPASS_FIR4X		BYPASS_FIR2X
0x38	56	AUTOMUTE ENABLE	AUTOMUTE_EN_CH8	AUTOMUTE_EN_CH7	AUTOMUTE_EN_CH6	AUTOMUTE_EN_CH5	AUTOMUTE_EN_CH4	AUTOMUTE_EN_CH3	AUTOMUTE_EN_CH2	AUTOMUTE_EN_CH1	
0x39	57	AUTOMUTE TIME	AUTOMUTE_TIME								
0x3A	58	AUTOMUTE TIME	RESERVED					AUTOMUTE_RAMP_TO_GROUND	AUTOMUTE_TIME		
0x3B	59	AUTOMUTE LEVEL	AUTOMUTE_LEVEL								
0x3C	60	AUTOMUTE LEVEL	AUTOMUTE_LEVEL								
0x3D	61	AUTOMUTE OFF LEVEL	AUTOMUTE_OFF_LEVEL								
0x3E	62	AUTOMUTE OFF LEVEL	AUTOMUTE_OFF_LEVEL								
0x3F	63	SOFT RAMP CONFIG	RESERVED				SOFT_RAMP_TIME				
0x40 - 0x41	64 - 65	RESERVED	RESERVED								
0xE0	224	SYS READ	RESERVED				MODES		ADDR1	ADDR0	
0xE1	225	CHIP ID READ	CHIP_ID								
0xE2 - 0xE4	226 - 228	RESERVED	RESERVED								
0xE5	229	RATIO VALID READ	RATIO_VALID	RESERVED							
0xE6	230	INPUT READBACK	RESERVED	TDM_DATA_VALID	DOP_VALID			INPUT_SELECT_OVERRIDE			
0xE7 - 0xE9	231 - 233	RESERVED	RESERVED								



## Register Listings

Some reserved registers values might be asserted in default mode. This is normal and does not need to be changed.

### System Registers

**Register 0: SYSTEM CONFIG**

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	2'b00	1'b0	1'b1	1'b0	1'b0

Bits	Mnemonic	Description
[7]	SOFT_RESET	Performs a soft reset to the digital core. <ul style="list-style-type: none"> <li>1'b0: Normal operation</li> <li>1'b1: Reset digital core (all settings are set to default)</li> </ul>
[6]	ENABLE_64FS_MODE	Enables 64FS mode to run the DAC interpolation path at 64FS. <ul style="list-style-type: none"> <li>1'b0: 64FS mode disabled (default)</li> <li>1'b1: 64FS mode enabled</li> </ul> Note: This mode should be used for high sample rates (i.e., 705.6/768 kHz)
[5]	RESERVED	NA
[4]	ENABLE_DOP_DECODE	Enables DoP decoding. <ul style="list-style-type: none"> <li>1'b0: Disabled (default)</li> <li>1'b1: Enabled</li> </ul>
[3]	ENABLE_DSD_DECODE	Enables DSD decoding. <ul style="list-style-type: none"> <li>1'b0: Disabled (default)</li> <li>1'b1: Enabled</li> </ul>
[2]	ENABLE_TDM_DECODE	Enables TDM decoding. <ul style="list-style-type: none"> <li>1'b0: Disabled</li> <li>1'b1: Enabled (default)</li> </ul>
[1]	DAC_MODE_REG	Enables DAC data path <ul style="list-style-type: none"> <li>1'b0: DAC disabled</li> <li>1'b1: DAC enabled</li> </ul>
[0]	RESERVED	NA

**Register 1: SYS MODE CONFIG**

Bits	[7:6]	[5]	[4:0]	[3:0]
Default	2'b00	1'b1	1'b1	4'b1000

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5]	ENABLE_DAC_CLK	Enables DAC interpolation path clock. <ul style="list-style-type: none"> <li>1'b0: Clock disabled</li> <li>1'b1: Clock enabled (default)</li> </ul>
[4]	ENABLE_NSMOD_CLK	Enables clock to the DAC
[3:0]	RESERVED	NA

## Register 2: DAC CLOCK CONFIG

Bits	[7]	[6]	[5:0]
Default	1'b1	1'b0	6'd0

Bits	Mnemonic	Description
[7]	AUTO_FS_DETECT	<ul style="list-style-type: none"> <li>1'b0: Disabled</li> <li>1'b1: Auto tune CLK_DAC/CLK_IDAC ratio according to detected FS (default)</li> </ul>
[6]	SELECT_IDAC_HALF	<ul style="list-style-type: none"> <li>1'b0: Divide by SELECT_IDAC_NUM + 1 (default)</li> <li>1'b1: Divide by half of SELECT_IDAC_NUM + 1</li> </ul> <p>Note: Can only produce half of an odd number divide</p>
[5:0]	SELECT_IDAC_NUM	<p>CLK_IDAC divider. Whole number divide value + 1 for CLK_IDAC (SYS_CLK/divide_value).</p> <ul style="list-style-type: none"> <li>6'd0: Whole number divide value + 1 = 1</li> <li>6'd1: Whole number divide value + 1 = 2</li> <li>6'd63: Whole number divide value + 1 = 64</li> </ul>

## Register 3: CLOCK CONFIG

Bits	[7:0]
Default	8'd7

Bits	Mnemonic	Description
[7:0]	MASTER_BCK_DIV	Master mode clock divider. Whole number divide value + 1 for CLK_Master (SYS_CLK/divide_value).

## Register 4: CONFIG

Bits	[7:6]	[5:4]	[3]	[2]	[1:0]
Default	2'b00	2'd0	1'b0	1'b0	2'b00

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5:4]	SEL_CLK	<p>Clock Gearing</p> <ul style="list-style-type: none"> <li>2'd0: SYS_CLK/1</li> <li>2'd1: SYS_CLK/2</li> <li>2'd2: SYS_CLK/4</li> <li>2'd3: SYS_CLK/8</li> </ul>
[3]	RESERVED	NA
[2]	AUTO_CLK_GEAR	<ul style="list-style-type: none"> <li>1'b0: Disable automatic clock gearing. SEL_CLK = sel_clk_reg</li> <li>1'b1: Enable automatic clock gearing. SEL_CLK will increase up to sel_clk_reg</li> </ul>
[1:0]	RESERVED	NA

## Register 15-6: RESERVED



## GPIO Registers

## Register 16: GPIO1/2 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd13

Bits	Mnemonic	Description
[7:4]	GPIO2_CFG	Configures GPIO2 <ul style="list-style-type: none"> <li>• 4'd0: Analog shutdown — shutdown</li> <li>• 4'd1: Output 0 — output</li> <li>• 4'd2: Output 1 — output</li> <li>• 4'd3: CLK_IDAC — output</li> <li>• 4'd4: Reserved</li> <li>• 4'd5: Mute all channels — input</li> <li>• 4'd6: Input selection — input</li> <li>• 4'd7: Lock status — output</li> <li>• 4'd8: CLK_VALID — output</li> <li>• 4'd9: TDM_VALID — output</li> <li>• 4'd10: DOP_VALID — output</li> <li>• 4'd11: BCK_WS_FAIL — output</li> <li>• 4'd12: Volume min — output</li> <li>• 4'd13: Automute status — output</li> <li>• 4'd14: Soft ramp finished — output</li> <li>• 4'd15: Reserved</li> </ul>
[3:0]	GPIO1_CFG	Configures GPIO1 <ul style="list-style-type: none"> <li>• 4'd0: Analog shutdown — shutdown</li> <li>• 4'd1: Output 0 — output</li> <li>• 4'd2: Output 1 — output</li> <li>• 4'd3: CLK_IDAC — output</li> <li>• 4'd4: Reserved</li> <li>• 4'd5: Mute all channels — input</li> <li>• 4'd6: Input selection — input</li> <li>• 4'd7: Lock status — output</li> <li>• 4'd8: CLK_VALID — output</li> <li>• 4'd9: TDM_VALID — output</li> <li>• 4'd10: DOP_VALID — output</li> <li>• 4'd11: BCK_WS_FAIL — output</li> <li>• 4'd12: Volume min — output</li> <li>• 4'd13: Automute status — output (default)</li> <li>• 4'd14: Soft ramp finished — output</li> <li>• 4'd15: Reserved</li> </ul>

## Register 17: GPIO3/4 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO4_CFG	Configures GPIO4 <ul style="list-style-type: none"> <li>• 4'd0: Analog shutdown — shutdown</li> <li>• 4'd1: Output 0 — output</li> <li>• 4'd2: Output 1 — output</li> <li>• 4'd3: CLK_IDAC — output</li> <li>• 4'd4: Reserved</li> <li>• 4'd5: Mute all channels — input</li> <li>• 4'd6: Input selection — input</li> <li>• 4'd7: Lock status — output</li> <li>• 4'd8: CLK_VALID — output</li> <li>• 4'd9: TDM_VALID — output</li> <li>• 4'd10: DOP_VALID — output</li> <li>• 4'd11: BCK_WS_FAIL — output</li> <li>• 4'd12: Volume min — output</li> <li>• 4'd13: Automute status — output</li> <li>• 4'd14: Soft ramp finished — output</li> <li>• 4'd15: Reserved</li> </ul>
[3:0]	GPIO3_CFG	Configures GPIO3 <ul style="list-style-type: none"> <li>• 4'd0: Analog shutdown — shutdown</li> <li>• 4'd1: Output 0 — output</li> <li>• 4'd2: Output 1 — output</li> <li>• 4'd3: CLK_IDAC — output</li> <li>• 4'd4: Reserved</li> <li>• 4'd5: Mute all channels — input</li> <li>• 4'd6: Input selection — input</li> <li>• 4'd7: Lock status — output</li> <li>• 4'd8: CLK_VALID — output</li> <li>• 4'd9: TDM_VALID — output</li> <li>• 4'd10: DOP_VALID — output</li> <li>• 4'd11: BCK_WS_FAIL — output</li> <li>• 4'd12: Volume min — output</li> <li>• 4'd13: Automute status — output</li> <li>• 4'd14: Soft ramp finished — output</li> <li>• 4'd15: Reserved</li> </ul>



## Register 18: GPIO5/6 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO6_CFG	Configures GPIO6 <ul style="list-style-type: none"> <li>• 4'd0: Analog shutdown — shutdown</li> <li>• 4'd1: Output 0 — output</li> <li>• 4'd2: Output 1 — output</li> <li>• 4'd3: CLK_IDAC — output</li> <li>• 4'd4: Reserved</li> <li>• 4'd5: Mute all channels — input</li> <li>• 4'd6: Input selection — input</li> <li>• 4'd7: Lock status — output</li> <li>• 4'd8: CLK_VALID — output</li> <li>• 4'd9: TDM_VALID — output</li> <li>• 4'd10: DOP_VALID — output</li> <li>• 4'd11: BCK_WS_FAIL — output</li> <li>• 4'd12: Volume min — output</li> <li>• 4'd13: Automute status — output</li> <li>• 4'd14: Soft ramp finished — output</li> <li>• 4'd15: Reserved</li> </ul>
[3:0]	GPIO5_CFG	Configures GPIO5 <ul style="list-style-type: none"> <li>• 4'd0: Analog shutdown — shutdown</li> <li>• 4'd1: Output 0 — output</li> <li>• 4'd2: Output 1 — output</li> <li>• 4'd3: CLK_IDAC — output</li> <li>• 4'd4: Reserved</li> <li>• 4'd5: Mute all channels — input</li> <li>• 4'd6: Input selection — input</li> <li>• 4'd7: Lock status — output</li> <li>• 4'd8: CLK_VALID — output</li> <li>• 4'd9: TDM_VALID — output</li> <li>• 4'd10: DOP_VALID — output</li> <li>• 4'd11: BCK_WS_FAIL — output</li> <li>• 4'd12: Volume min — output</li> <li>• 4'd13: Automute status — output</li> <li>• 4'd14: Soft ramp finished — output</li> <li>• 4'd15: Reserved</li> </ul>



## Register 19: GPIO7/8 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO8_CFG	Configures GPIO8 <ul style="list-style-type: none"> <li>• 4'd0: Analog shutdown — shutdown</li> <li>• 4'd1: Output 0 — output</li> <li>• 4'd2: Output 1 — output</li> <li>• 4'd3: CLK_IDAC — output</li> <li>• 4'd4: Reserved</li> <li>• 4'd5: Mute all channels — input</li> <li>• 4'd6: Input selection — input</li> <li>• 4'd7: Lock status — output</li> <li>• 4'd8: CLK_VALID — output</li> <li>• 4'd9: TDM_VALID — output</li> <li>• 4'd10: DOP_VALID — output</li> <li>• 4'd11: BCK_WS_FAIL — output</li> <li>• 4'd12: Volume min — output</li> <li>• 4'd13: Automute status — output</li> <li>• 4'd14: Soft ramp finished — output</li> <li>• 4'd15: Reserved</li> </ul>
[3:0]	GPIO7_CFG	Configures GPIO7 <ul style="list-style-type: none"> <li>• 4'd0: Analog shutdown — shutdown</li> <li>• 4'd1: Output 0 — output</li> <li>• 4'd2: Output 1 — output</li> <li>• 4'd3: CLK_IDAC — output</li> <li>• 4'd4: Reserved</li> <li>• 4'd5: Mute all channels — input</li> <li>• 4'd6: Input selection — input</li> <li>• 4'd7: Lock status — output</li> <li>• 4'd8: CLK_VALID — output</li> <li>• 4'd9: TDM_VALID — output</li> <li>• 4'd10: DOP_VALID — output</li> <li>• 4'd11: BCK_WS_FAIL — output</li> <li>• 4'd12: Volume min — output</li> <li>• 4'd13: Automute status — output</li> <li>• 4'd14: Soft ramp finished — output</li> <li>• 4'd15: Reserved</li> </ul>



## Register 20: GPIO OUTPUT ENABLE

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b1

Bits	Mnemonic	Description
[7]	GPIO8_OE	<ul style="list-style-type: none"> <li>1'b0: Tristate GPIO8 (default)</li> <li>1'b1: GPIO8 Output Enable</li> </ul>
[6]	GPIO7_OE	<ul style="list-style-type: none"> <li>1'b0: Tristate GPIO7 (default)</li> <li>1'b1: GPIO7 Output Enable</li> </ul>
[5]	GPIO6_OE	<ul style="list-style-type: none"> <li>1'b0: Tristate GPIO6 (default)</li> <li>1'b1: GPIO6 Output Enable</li> </ul>
[4]	GPIO5_OE	<ul style="list-style-type: none"> <li>1'b0: Tristate GPIO5 (default)</li> <li>1'b1: GPIO5 Output Enable</li> </ul>
[3]	GPIO4_OE	<ul style="list-style-type: none"> <li>1'b0: Tristate GPIO4 (default)</li> <li>1'b1: GPIO4 Output Enable</li> </ul>
[2]	GPIO3_OE	<ul style="list-style-type: none"> <li>1'b0: Tristate GPIO3 (default)</li> <li>1'b1: GPIO3 Output Enable</li> </ul>
[1]	GPIO2_OE	<ul style="list-style-type: none"> <li>1'b0: Tristate GPIO2 (default)</li> <li>1'b1: GPIO2 Output Enable</li> </ul>
[0]	GPIO1_OE	<ul style="list-style-type: none"> <li>1'b0: Tristate GPIO1</li> <li>1'b1: GPIO1 Output Enable (default)</li> </ul>

## Register 21: GPIO INPUT

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b1	1'b1	1'b1	1'b0	1'b0

Bits	Mnemonic	Description
[7]	GPIO8_SDB	<ul style="list-style-type: none"> <li>1'b0: Disables GPIO8 input (default)</li> <li>1'b1: Enables GPIO8 input</li> </ul>
[6]	GPIO7_SDB	<ul style="list-style-type: none"> <li>1'b0: Disables GPIO7 input (default)</li> <li>1'b1: Enables GPIO7 input</li> </ul>
[5]	GPIO6_SDB	<ul style="list-style-type: none"> <li>1'b0: Disables GPIO6 input (default)</li> <li>1'b1: Enables GPIO6 input</li> </ul>
[4]	GPIO5_SDB	<ul style="list-style-type: none"> <li>1'b0: Disables GPIO5 input</li> <li>1'b1: Enables GPIO5 input (default)</li> </ul>
[3]	GPIO4_SDB	<ul style="list-style-type: none"> <li>1'b0: Disables GPIO4 input</li> <li>1'b1: Enables GPIO4 input (default)</li> </ul>
[2]	GPIO3_SDB	<ul style="list-style-type: none"> <li>1'b0: Disables GPIO3 input</li> <li>1'b1: Enables GPIO3 input (default)</li> </ul>
[1]	GPIO2_SDB	<ul style="list-style-type: none"> <li>1'b0: Disables GPIO2 input (default)</li> <li>1'b1: Enables GPIO2 input</li> </ul>
[0]	GPIO1_SDB	<ul style="list-style-type: none"> <li>1'b0: Disables GPIO1 input (default)</li> <li>1'b1: Enables GPIO1 input</li> </ul>

## Register 22: RESERVED

## Register 24-23: GPIO OUTPUT LOGIC

Bits	[15]	[14:9]	[8:6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	6'd0	3'd0	1'b0	1'b0	1'b0	1'b1	1'b1	1'b1

Bits	Mnemonic	Description
[15]	GPIO_DAC_MODE	When any GPIOx_CFG = 6 (input system mode control): <ul style="list-style-type: none"> <li>1'b0: Power down when GPIO input is 1</li> <li>1'b1: HIFI when GPIO input is 1 (when GPIO input is 0, system mode is determined by register DAC_MODE_REG (register 0, bit[1]))</li> </ul>
[14:9]	RESERVED	NA
[8:6]	GPIO_SEL	When GPIOx_CFG = 12, 13 or 14, and the corresponding GPIO_AND and GPIO_OR are not set: <ul style="list-style-type: none"> <li>3'd0: Outputs status/flag from ch1</li> <li>3'd1: Outputs status/flag from ch2</li> <li>3'd2: Outputs status/flag from ch3</li> <li>3'd3: Outputs status/flag from ch4</li> <li>3'd4: Outputs status/flag from ch5</li> <li>3'd5: Outputs status/flag from ch6</li> <li>3'd6: Outputs status/flag from ch7</li> <li>3'd7: Outputs status/flag from ch8</li> </ul>
[5]	GPIO_OR_SS_RAMP	When GPIOx_CFG = 14 (output soft ramp done flag): <ul style="list-style-type: none"> <li>1'b0: The soft ramp done flag is determined by GPIO_AND_SS_RAMP and GPIO_SEL (default)</li> <li>1'b1: The soft ramp done flag is the "OR" of all 8ch soft ramp done flags</li> </ul>
[4]	GPIO_OR_VOL_MIN	When GPIOx_CFG = 12 (output vol_min flag): <ul style="list-style-type: none"> <li>1'b0: The vol_min flag is determined by GPIO_AND_VOL_MIN and GPIO_SEL (default)</li> <li>1'b1: The vol_min flag is the "OR" of all 8ch vol_min flags</li> </ul>
[3]	GPIO_OR_AUTOMUTE	When GPIOx_CFG = 13 (output automute status): <ul style="list-style-type: none"> <li>1'b0: The automute status is determined by GPIO_AND_AUTOMUTE and GPIO_SEL (default)</li> <li>1'b1: The automute status is the "OR" of all 8ch automute status</li> </ul>
[2]	GPIO_AND_SS_RAMP	When GPIOx_CFG = 14 (output soft ramp done flag) and GPIO_OR_SS_RAMP is not set: <ul style="list-style-type: none"> <li>1'b0: The soft ramp done flag is from a single channel selected by GPIO_SEL</li> <li>1'b1: The soft ramp done flag is the "AND" of all 8ch soft ramp done flags (default)</li> </ul>
[1]	GPIO_AND_VOL_MIN	When GPIOx_CFG = 12 (output vol_min flag) and GPIO_OR_VOL_MIN is not set: <ul style="list-style-type: none"> <li>1'b0: The vol_min flag is from a single channel selected by GPIO_SEL</li> <li>1'b1: The vol_min flag is the "AND" of all 8ch vol_min flags (default)</li> </ul>
[0]	GPIO_AND_AUTOMUTE	When GPIOx_CFG = 13 (output automute status) and GPIO_OR_AUTOMUTE is not set: <ul style="list-style-type: none"> <li>1'b0: The automute status is from a single channel selected by GPIO_SEL</li> <li>1'b1: The automute status is the "AND" of all 8ch automute status (default)</li> </ul>



## DAC Registers

### Register 25: INPUT SELECTION

Bits	[7]	[6]	[5]	[4]	[3]	[2:1]	[0]
Default	1'b0	1'b1	1'b0	1'b0	1'b0	2'd0	1'b0

Bits	Mnemonic	Description
[7]	AUTO_CH_DETECT	Auto detect BCK/FRAME ratio to determine the number of TDM channels <ul style="list-style-type: none"> <li>1'b0: Disabled (default)</li> <li>1'b1: Enabled</li> </ul>
[6]	ENABLE_DSD_FAULT_DETECTION	<ul style="list-style-type: none"> <li>1'b0: Disabled</li> <li>1'b1: Enabled (default)</li> </ul>
[5]	DSD_MASTER_MODE	DSD master mode config. <ul style="list-style-type: none"> <li>1'b0: DSD slave mode (default)</li> <li>1'b1: DSD master mode. DSD_CLK outputs from DATA_CLK</li> </ul>
[4]	PCM_MASTER_MODE	PCM master mode config. <ul style="list-style-type: none"> <li>1'b0: PCM slave mode (default)</li> <li>1'b1: PCM master mode enabled. Master BCK and WS output from DATA_CLK and DATA1</li> </ul>
[3]	RESERVED	NA
[2:1]	INPUT_SEL	Selects input data when AUTO_INPUT_SELECT is disabled. <ul style="list-style-type: none"> <li>2'd0: TDM (default)</li> <li>2'd1: DSD</li> <li>2'd2: DoP</li> <li>2'd3: Reserved</li> </ul>
[0]	AUTO_INPUT_SEL	Automatic input data selection config. <ul style="list-style-type: none"> <li>1'b0: Disables auto input select. Input data format is set by INPUT_SEL (default)</li> <li>1'b1: Automatically determine the input data format.</li> </ul>

## Register 26: SERIAL MASTER ENCODER CONFIG

Bits	[7]	[6]	[5]	[4:3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	2'd0	1'b0	1'b0	1'b1

Bits	Mnemonic	Description
[7]	TDM_RESYNC	Force TDM decoder to resync. <ul style="list-style-type: none"> <li>1'b0: Let decoder sync (default)</li> <li>1'b1: Force decoder not sync</li> </ul>
[6]	BCK_INV	Invert the slave BCK <ul style="list-style-type: none"> <li>1'b0: Normal operation</li> <li>1'b1: Invert slave BCK</li> </ul>
[5]	RESERVED	NA
[4:3]	MASTER_FRAME_LENGTH	Selects the bit length in each TDM channel in master mode. <ul style="list-style-type: none"> <li>2'd0: 32-bit (default)</li> <li>2'd2: 16-bit</li> <li>others: Reserved</li> </ul>
[2]	MASTER_WS_PULSE_MODE	When enabled, master WS is a pulse signal instead of a 50% duty cycle signal. The pulse width is 1 BCK cycle. <ul style="list-style-type: none"> <li>1'b0: 50% duty cycle WS signal (default)</li> <li>1'b1: Pulse WS signal</li> </ul>
[1]	MASTER_WS_INVERT	Inverts master WS. <ul style="list-style-type: none"> <li>1'b0: Non-inverted (default)</li> <li>1'b1: Inverted</li> </ul>
[0]	MASTER_BCK_INVERT	Inverts master BCK or DSD_CLK. <ul style="list-style-type: none"> <li>1'b0: Non-inverted</li> <li>1'b1: Inverted (default)</li> </ul>

## Register 27: TDM CONFIG

Bits	[7:5]	[4:0]
Default	3'd0	5'd1

Bits	Mnemonic	Description
[7:5]	RESERVED	NA
[4:0]	TDM_CH_NUM	Total number of TDM slots per frame = TDM_CH_NUM + 1.

## Register 28: TDM CONFIG1

Bits	[7]	[6]	[5:0]
Default	1'b0	1'b0	6'd0

Bits	Mnemonic	Description
[7]	TDM_LJ_MODE	TDM LJ mode. <ul style="list-style-type: none"> <li>1'b0: Standard I2S (default)</li> <li>1'b1: LJ mode</li> </ul>
[6]	TDM_VALID_EDGE	TDM WS valid edge. <ul style="list-style-type: none"> <li>1'b0: negative edge (default)</li> <li>1'b1: positive edge</li> </ul>
[5:0]	RESERVED	NA



## Register 29: TDM CONFIG2

Bits	[7]	[6:5]	[4:0]
Default	1'b1	2'b00	5'd0

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6:5]	TDM_BIT_WIDTH	Bit width of each TDM slot. <ul style="list-style-type: none"> <li>2'b00: 32-bit (default)</li> <li>2'b01: 24-bit</li> <li>2'b10: 16-bit</li> <li>2'b11: Reserved</li> </ul>
[4:0]	TDM_DATA_LATCH_ADJ	Sets the position of the start bit within each TDM slot. Can be moved by TDM_DATA_LATCH_ADJ clock cycles. <ul style="list-style-type: none"> <li>5'd0: Normal position</li> <li>5'd1-31: Number of clock cycles to wait</li> </ul> Note: This value does not work in LJ mode

## Register 30: BCK/WS MONITOR CONFIG

Bits	[7]	[6]	[5]	[4]	[3]	[2:0]
Default	1'b0	1'b0	1'b1	1'b1	1'b0	3'd0

Bits	Mnemonic	Description
[7]	DISABLE_DSD_DC	<ul style="list-style-type: none"> <li>1'b0: DSD DC can trigger an automute if automute is enabled (default)</li> <li>1'b1: DSD DC is ignored.</li> </ul>
[6]	DISABLE_DSD_MUTE	<ul style="list-style-type: none"> <li>1'b0: DSD mute pattern can trigger an automute is automute is enabled (default)</li> <li>1'b1: DSD mute pattern is ignored.</li> </ul>
[5]	ENABLE_WS_MONITOR	Enable WS monitor. <ul style="list-style-type: none"> <li>1'b0: Disable</li> <li>1'b1: Enable (default)</li> </ul>
[4]	ENABLE_BCK_MONITOR	Enable BCK monitor. <ul style="list-style-type: none"> <li>1'b0: Disable (default)</li> <li>1'b1: Enable</li> </ul>
[3]	DISABLE_PCM_DC	<ul style="list-style-type: none"> <li>1'b0: PCM DC signal can trigger an automute if automute is enabled.</li> <li>1'b1: PCM DC is ignored.</li> </ul>
[2:0]	RESERVED	NA

## Register 31: RESERVED

## Register 32: TDM CH1 CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd0	5'd0

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6:5]	TDM_CH1_LINE_SEL	CH1 data line selection. CH1 receives data from data line. <ul style="list-style-type: none"> <li>2d'0 = DATA1</li> <li>2d'1 = DATA2</li> <li>2d'2 = DATA3</li> <li>2d'3 = DATA4</li> </ul> Note: Valid for TDM, PCM and DoP.
[4:0]	TDM_CH1_SLOT_SEL	CH1 data slot selection. CH1 receives data from Mth slot. M = TDM_CH1_SLOT_SEL + 1. Note: Valid for TDM, PCM and DoP.

## Register 33: TDM CH2 CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd0	5'd1

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6:5]	TDM_CH2_LINE_SEL	CH2 data line selection. CH2 receives data from data line. <ul style="list-style-type: none"> <li>2d'0 = DATA1</li> <li>2d'1 = DATA2</li> <li>2d'2 = DATA3</li> <li>2d'3 = DATA4</li> </ul> Note: Valid for TDM, PCM and DoP.
[4:0]	TDM_CH2_SLOT_SEL	CH2 data slot selection. CH2 receives data from Mth slot. M = TDM_CH2_SLOT_SEL + 1. Note: Valid for TDM, PCM and DoP.

## Register 34: TDM CH3 CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd1	5'd0

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6:5]	TDM_CH3_LINE_SEL	CH3 data line selection. CH3 receives data from data line. <ul style="list-style-type: none"> <li>2d'0 = DATA1</li> <li>2d'1 = DATA2</li> <li>2d'2 = DATA3</li> <li>2d'3 = DATA4</li> </ul> Note: Valid for TDM, PCM and DoP.
[4:0]	TDM_CH3_SLOT_SEL	CH3 data slot selection. CH3 receives data from Mth slot. M = TDM_CH3_SLOT_SEL + 1. Note: Valid for TDM, PCM and DoP.



## Register 35: TDM CH4 CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd1	5'd1

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6:5]	TDM_CH4_LINE_SEL	CH4 data line selection. CH4 receives data from data line. <ul style="list-style-type: none"> <li>• 2d'0 = DATA1</li> <li>• 2d'1 = DATA2</li> <li>• 2d'2 = DATA3</li> <li>• 2d'3 = DATA4</li> </ul> Note: Valid for TDM, PCM and DoP.
[4:0]	TDM_CH4_SLOT_SEL	CH4 data slot selection. CH4 receives data from Mth slot. M = TDM_CH4_SLOT_SEL + 1. Note: Valid for TDM, PCM and DoP.

## Register 36: TDM CH5 CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd2	5'd0

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6:5]	TDM_CH5_LINE_SEL	CH5 data line selection. CH5 receives data from data line. <ul style="list-style-type: none"> <li>• 2d'0 = DATA1</li> <li>• 2d'1 = DATA2</li> <li>• 2d'2 = DATA3</li> <li>• 2d'3 = DATA4</li> </ul> Note: Valid for TDM, PCM and DoP.
[4:0]	TDM_CH5_SLOT_SEL	CH5 data slot selection. CH5 receives data from Mth slot. M = TDM_CH5_SLOT_SEL + 1. Note: Valid for TDM, PCM and DoP.

## Register 37: TDM CH6 CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd2	5'd1

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6:5]	TDM_CH6_LINE_SEL	CH6 data line selection. CH6 receives data from data line. <ul style="list-style-type: none"> <li>• 2d'0 = DATA1</li> <li>• 2d'1 = DATA2</li> <li>• 2d'2 = DATA3</li> <li>• 2d'3 = DATA4</li> </ul> Note: Valid for TDM, PCM and DoP.
[4:0]	TDM_CH6_SLOT_SEL	CH6 data slot selection. CH6 receives data from Mth slot. M = TDM_CH6_SLOT_SEL + 1. Note: Valid for TDM, PCM and DoP.



## Register 38: TDM CH7 CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd3	5'd0

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6:5]	TDM_CH7_LINE_SEL	CH7 data line selection. CH7 receives data from data line. <ul style="list-style-type: none"> <li>2d'0 = DATA1</li> <li>2d'1 = DATA2</li> <li>2d'2 = DATA3</li> <li>2d'3 = DATA4</li> </ul> Note: Valid for TDM, PCM and DoP.
[4:0]	TDM_CH7_SLOT_SEL	CH7 data slot selection. CH7 receives data from Mth slot. M = TDM_CH7_SLOT_SEL + 1. Note: Valid for TDM, PCM and DoP.

## Register 39: TDM CH8 CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd3	5'd1

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6:5]	TDM_CH8_LINE_SEL	CH8 data line selection. CH8 receives data from data line. <ul style="list-style-type: none"> <li>2d'0 = DATA1</li> <li>2d'1 = DATA2</li> <li>2d'2 = DATA3</li> <li>2d'3 = DATA4</li> </ul> Note: Valid for TDM, PCM and DoP.
[4:0]	TDM_CH8_SLOT_SEL	CH8 data slot selection. CH8 receives data from Mth slot. M = TDM_CH8_SLOT_SEL + 1. Note: Valid for TDM, PCM and DoP.

## Register 40: VOLUME1

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME1	DAC ch1 volume. -0dB to -127.5dB 0.5dB steps. <ul style="list-style-type: none"> <li>8'd0: 0dB</li> <li>8'd255: -127.5dB</li> </ul>

## Register 41: VOLUME2

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME2	DAC ch2 volume. -0dB to -127.5dB 0.5dB steps. <ul style="list-style-type: none"> <li>8'd0: 0dB</li> <li>8'd255: -127.5dB</li> </ul>

**Register 42: VOLUME3**

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME3	DAC ch3 volume. -0dB to -127.5dB 0.5dB steps. <ul style="list-style-type: none"> <li>8'd0: 0dB</li> <li>8'd255: -127.5dB</li> </ul>

**Register 43: VOLUME4**

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME4	DAC ch4 volume. -0dB to -127.5dB 0.5dB steps. <ul style="list-style-type: none"> <li>8'd0: 0dB</li> <li>8'd255: -127.5dB</li> </ul>

**Register 44: VOLUME5**

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME5	DAC ch5 volume. -0dB to -127.5dB 0.5dB steps. <ul style="list-style-type: none"> <li>8'd0: 0dB</li> <li>8'd255: -127.5dB</li> </ul>

**Register 45: VOLUME6**

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME6	DAC ch6 volume. -0dB to -127.5dB 0.5dB steps. <ul style="list-style-type: none"> <li>8'd0: 0dB</li> <li>8'd255: -127.5dB</li> </ul>

**Register 46: VOLUME7**

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME7	DAC ch7 volume. -0dB to -127.5dB 0.5dB steps. <ul style="list-style-type: none"> <li>8'd0: 0dB</li> <li>8'd255: -127.5dB</li> </ul>

## Register 47: VOLUME8

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME8	DAC ch8 volume. -0dB to -127.5dB 0.5dB steps. <ul style="list-style-type: none"> <li>8'd0: 0dB</li> <li>8'd255: -127.5dB</li> </ul>

## Register 48: DAC VOL UP RATE

Bits	[7:0]
Default	8'd4

Bits	Mnemonic	Description
[7:0]	DAC_VOL_RATE_UP	Value by which the old VOLUME value is incremented to reach the new VOLUME value Valid from 8'd0 (instant) to 8'd255 (fastest), where 8'd0 instantly changes the VOLUME value <ul style="list-style-type: none"> <li>8'd0: Instant change</li> <li>8'd4: Default</li> <li>8'd255: Fastest change</li> </ul> $ramp\_rate [s] = \frac{2^{15}}{DAC\_VOL\_RATE\_UP * FS}$

## Register 49: DAC VOL DOWN RATE

Bits	[7:0]
Default	8'd4

Bits	Mnemonic	Description
[7:0]	DAC_VOL_RATE_DOWN	Value by which the old VOLUME value is incremented to reach the new VOLUME value Valid from 8'd0 (instant) to 8'd255 (fastest), where 8'd0 instantly changes the VOLUME value <ul style="list-style-type: none"> <li>8'd0: Instant change</li> <li>8'd4: Default</li> <li>8'd255: Fastest change</li> </ul> $ramp\_rate [s] = \frac{2^{15}}{DAC\_VOL\_RATE\_DOWN * FS}$



## Register 50: DAC VOL DOWN RATE FAST

Bits	[7:0]
Default	8'd255

Bits	Mnemonic	Description
[7:0]	DAC_VOL_RATE_FAST	<p>Value by which the old VOLUME value is incremented to reach the new VOLUME value</p> <p>Valid from 8'd0 (instant) to 8'd255 (fastest), where 8'd0 instantly changes the VOLUME value</p> <p>Only used during abnormal mute (PLL unlock or BCK_WS ratio failed)</p> <ul style="list-style-type: none"> <li>8'd0: Instant change</li> <li>8'd255: Fastest change (default)</li> </ul> $ramp\_rate [s] = \frac{2^{15}}{DAC\_VOL\_RATE\_FAST * FS}$

## Register 51: DAC MUTE

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	DAC_MUTE_CH8	<ul style="list-style-type: none"> <li>1'b0: Normal operation (default)</li> <li>1'b1: Mute ch8</li> </ul>
[6]	DAC_MUTE_CH7	<ul style="list-style-type: none"> <li>1'b0: Normal operation (default)</li> <li>1'b1: Mute ch7</li> </ul>
[5]	DAC_MUTE_CH6	<ul style="list-style-type: none"> <li>1'b0: Normal operation (default)</li> <li>1'b1: Mute ch6</li> </ul>
[4]	DAC_MUTE_CH5	<ul style="list-style-type: none"> <li>1'b0: Normal operation (default)</li> <li>1'b1: Mute ch5</li> </ul>
[3]	DAC_MUTE_CH4	<ul style="list-style-type: none"> <li>1'b0: Normal operation (default)</li> <li>1'b1: Mute ch4</li> </ul>
[2]	DAC_MUTE_CH3	<ul style="list-style-type: none"> <li>1'b0: Normal operation (default)</li> <li>1'b1: Mute ch3</li> </ul>
[1]	DAC_MUTE_CH2	<ul style="list-style-type: none"> <li>1'b0: Normal operation (default)</li> <li>1'b1: Mute ch2</li> </ul>
[0]	DAC_MUTE_CH1	<ul style="list-style-type: none"> <li>1'b0: Normal operation (default)</li> <li>1'b1: Mute ch1</li> </ul>

## Register 52: DAC INVERT

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	DAC_INVERT_CH8	Invert the output on Ch8 at the input to the NSMOD
[6]	DAC_INVERT_CH7	Invert the output on Ch7 at the input to the NSMOD
[5]	DAC_INVERT_CH6	Invert the output on Ch6 at the input to the NSMOD
[4]	DAC_INVERT_CH5	Invert the output on Ch5 at the input to the NSMOD
[3]	DAC_INVERT_CH4	Invert the output on Ch4 at the input to the NSMOD
[2]	DAC_INVERT_CH3	Invert the output on Ch3 at the input to the NSMOD
[1]	DAC_INVERT_CH2	Invert the output on Ch2 at the input to the NSMOD
[0]	DAC_INVERT_CH1	Invert the output on Ch1 at the input to the NSMOD

## Register 53: FILTER SHAPE

Bits	[7:3]	[2:0]
Default	5'd12	3'd0

Bits	Mnemonic	Description
[7:3]	RESERVED	NA
[2:0]	FILTER_SHAPE	Selects the 8x interpolation FIR filter shape. <ul style="list-style-type: none"> <li>3'd0: Minimum phase (default)</li> <li>3'd1: Linear phase apodizing</li> <li>3'd2: Linear phase fast roll-off</li> <li>3'd4: Linear phase slow roll-off</li> <li>3'd5: Minimum phase fast roll-off</li> <li>3'd6: Minimum phase slow roll-off</li> <li>3'd7: Minimum phase slow roll-off low dispersion</li> </ul>

## Register 54: IIR BANDWIDTH

Bits	[7:4]	[3]	[2:0]
Default	4'd0	1'b0	3'd4

Bits	Mnemonic	Description
[7:4]	RESERVED	NA
[3]	VOLUME_HOLD	Hold volume coefficients to allow for all channels to update at same time
[2:0]	IIR_BW	Controls the IIR bandwidth in the digital datapath. <ul style="list-style-type: none"> <li>3'd0: Invalid</li> <li>3'd1: BW * 8</li> <li>3'd2: BW * 4</li> <li>3'd3: BW * 2</li> <li>3'd4: Default BW</li> <li>3'd5: BW / 2</li> <li>3'd6: BW / 4</li> <li>3'd7: BW / 8</li> </ul>



## Register 55: DAC PATH CONFIG

Bits	[7:2]	[1]	[0]
Default	6'b000000	1'b0	1'b0

Bits	Mnemonic	Description
[7:2]	RESERVED	NA
[1]	BYPASS_FIR4X	<ul style="list-style-type: none"> <li>1'b0: Non-bypass IFir_4x (default)</li> <li>1'b1: Bypass IFir_4x</li> </ul>
[0]	BYPASS_FIR2X	<ul style="list-style-type: none"> <li>1'b0: Non-bypass IFir_2x (default)</li> <li>1'b1: Bypass IFir_2x</li> </ul>

## Register 56: AUTOMUTE ENABLE

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b1	1'b1	1'b1	1'b1	1'b1	1'b1	1'b1	1'b1

Bits	Mnemonic	Description
[7]	AUTOMUTE_EN_CH8	<ul style="list-style-type: none"> <li>1'b0: Disables ch8 automute</li> <li>1'b1: Enables ch8 automute (default)</li> </ul> <p>Note: Automute is available for PCM only</p>
[6]	AUTOMUTE_EN_CH7	<ul style="list-style-type: none"> <li>1'b0: Disables ch7 automute</li> <li>1'b1: Enables ch7 automute (default)</li> </ul> <p>Note: Automute is available for PCM only</p>
[5]	AUTOMUTE_EN_CH6	<ul style="list-style-type: none"> <li>1'b0: Disables ch6 automute</li> <li>1'b1: Enables ch6 automute (default)</li> </ul> <p>Note: Automute is available for PCM only</p>
[4]	AUTOMUTE_EN_CH5	<ul style="list-style-type: none"> <li>1'b0: Disables ch5 automute</li> <li>1'b1: Enables ch5 automute (default)</li> </ul> <p>Note: Automute is available for PCM only</p>
[3]	AUTOMUTE_EN_CH4	<ul style="list-style-type: none"> <li>1'b0: Disables ch4 automute</li> <li>1'b1: Enables ch4 automute (default)</li> </ul> <p>Note: Automute is available for PCM only</p>
[2]	AUTOMUTE_EN_CH3	<ul style="list-style-type: none"> <li>1'b0: Disables ch3 automute</li> <li>1'b1: Enables ch3 automute (default)</li> </ul> <p>Note: Automute is available for PCM only</p>
[1]	AUTOMUTE_EN_CH2	<ul style="list-style-type: none"> <li>1'b0: Disables ch2 automute</li> <li>1'b1: Enables ch2 automute (default)</li> </ul> <p>Note: Automute is available for PCM only</p>
[0]	AUTOMUTE_EN_CH1	<ul style="list-style-type: none"> <li>1'b0: Disables ch1 automute</li> <li>1'b1: Enables ch1 automute (default)</li> </ul> <p>Note: Automute is available for PCM only</p>

## Register 58-57: AUTOMUTE TIME

Bits	[15:12]	[11]	[10:0]
Default	4'd0	1'b1	11'd15

Bits	Mnemonic	Description
[15:12]	RESERVED	NA
[11]	AUTOMUTE_RAMP_TO_GROUND	<ul style="list-style-type: none"> <li>1'b0: When ramped to min volume during normal mute, do not soft ramp to ground</li> <li>1'b1: When ramped to min volume during normal mute, soft ramp to ground for power saving (default)</li> </ul> <p>normal mute includes: automute, mute by register, mute by GPIO</p>
[10:0]	AUTOMUTE_TIME	<p>Configures the amount of time in seconds the audio must remain below AUTOMUTE_LEVEL before an automute condition is flagged.</p> <p>Valid from 0 (disabled) to 11'h7FF (fastest), where 11'h001 is the slowest</p> $Time (s) = \frac{2^{18}}{AUTOMUTE\_TIME * FS}$

## Register 60-59: AUTOMUTE LEVEL

Bits	[15:0]
Default	16'0008

Bits	Mnemonic	Description
[15:0]	AUTOMUTE_LEVEL	<p>Configures the threshold which the audio must be below before an automute condition is flagged.</p> <p>Valid from: 16'hFFFF (-42dB) to 16'h0002 (-132dB)</p> <p>Shift right 1 bit corresponds to -6dB</p> $20 \log_{10} \left( \frac{AUTOMUTE\_LEVEL}{2^{16} - 1} \right) - 42$ <p>Note: this register works in tandem with AUTOMUTE_TIME to create the automute condition</p>

## Register 62-61: AUTOMUTE OFF LEVEL

Bits	[15:0]
Default	16'000A

Bits	Mnemonic	Description
[15:0]	AUTOMUTE_OFF_LEVEL	<p>Configures the threshold which the audio must be above before the automute condition is cleared (cleared immediately).</p> <p>Valid from: 16'hFFFF (-42dB) to 16'h0002 (-132dB)</p> <p>Shift right 1 bit corresponds to -6dB</p> $20 \log_{10} \left( \frac{AUTOMUTE\_OFF\_LEVEL}{2^{16} - 1} \right) - 42$



## Register 63: SOFT RAMP CONFIG

Bits	[7:5]	[4:0]
Default	3'b110	5'd3

Bits	Mnemonic	Description
[7:5]	RESERVED	NA
[4:0]	SOFT_RAMP_TIME	<p>Sets the amount of time that it takes to perform a soft start ramp. This time affects both ramp to ground and ramp to AVCC/2. Valid from 0 to 20 (inclusive).</p> $Time [s] = \frac{4096 * 2^{(SOFT\_RAMP\_TIME+1)}}{CLK\_IDAC}$

## Register 65-64: RESERVED



## Readback Registers

### Register 224: SYS READ

Bits	[7:4]	[3:2]	[1]	[0]
Default	-	-	-	-

Bits	Mnemonic	Description
[7:4]	RESERVED	NA
[3:2]	MODES	Chip mode readback. Based on MODE Pin <ul style="list-style-type: none"> <li>• 2'd0: I2C</li> <li>• 2'd3: SPI</li> </ul> Note: All other values are invalid.
[1]	ADDR1	I2C address select bit 1.
[0]	ADDR0	I2C address select bit 0.

### Register 225: CHIP ID READ

Bits	[7:0]
Default	8'h60

Bits	Mnemonic	Description
[7:0]	CHIP_ID	CHIP ID.

### Register 228-227: RESERVED

### Register 229: RATIO VALID READ

Bits	[7]	[6:0]
Default	-	-

Bits	Mnemonic	Description
[7]	RATIO_VALID	Indicates validity of the CLK_DAC/CLK_IDAC ratio <ul style="list-style-type: none"> <li>• 1'b0: Invalid</li> <li>• 1'b1: Valid</li> </ul>
[6:0]	RESERVED	NA

### Register 230: INPUT READBACK

Bits	[7]	[6]	[5:2]	[1:0]
Default	-	-	-	-

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6]	TDM_DATA_VALID	TDM valid data flag
[5:2]	DOP_VALID	DoP valid flag
[1:0]	INPUT_SELECT_OVERRIDE	AUTO_INPUT_SEL value

## ES9017 Reference Schematics

### ES9017 Hardware (HW) mode

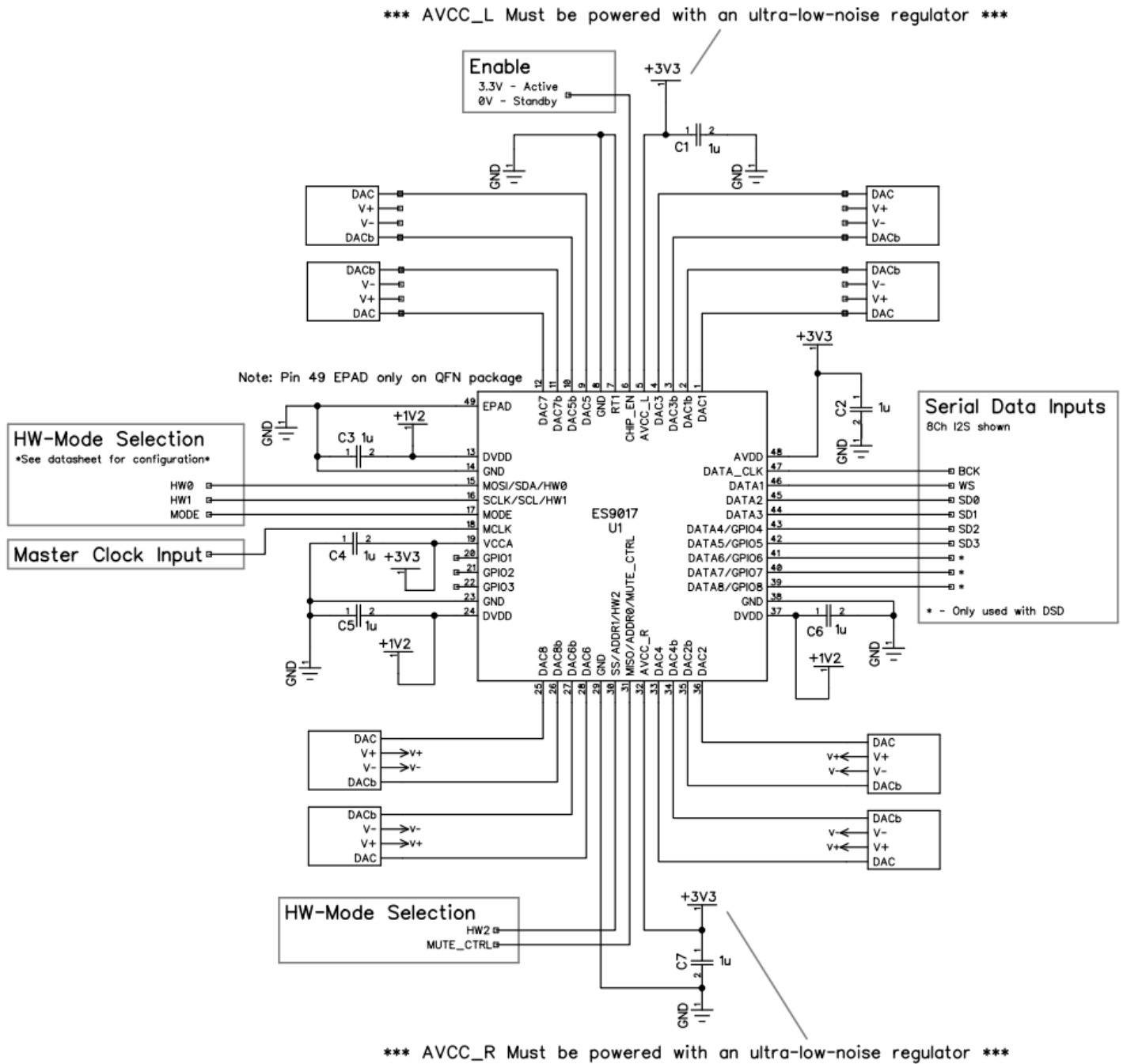


Figure 15 – Hardware (HW) mode reference schematic for ES9017Q

Note: ES9017Q has an exposed pad (EPAD, pin 49) and should be connected to ground. ES9017S does not have an exposed pad.

ES9017 Software (SW) mode

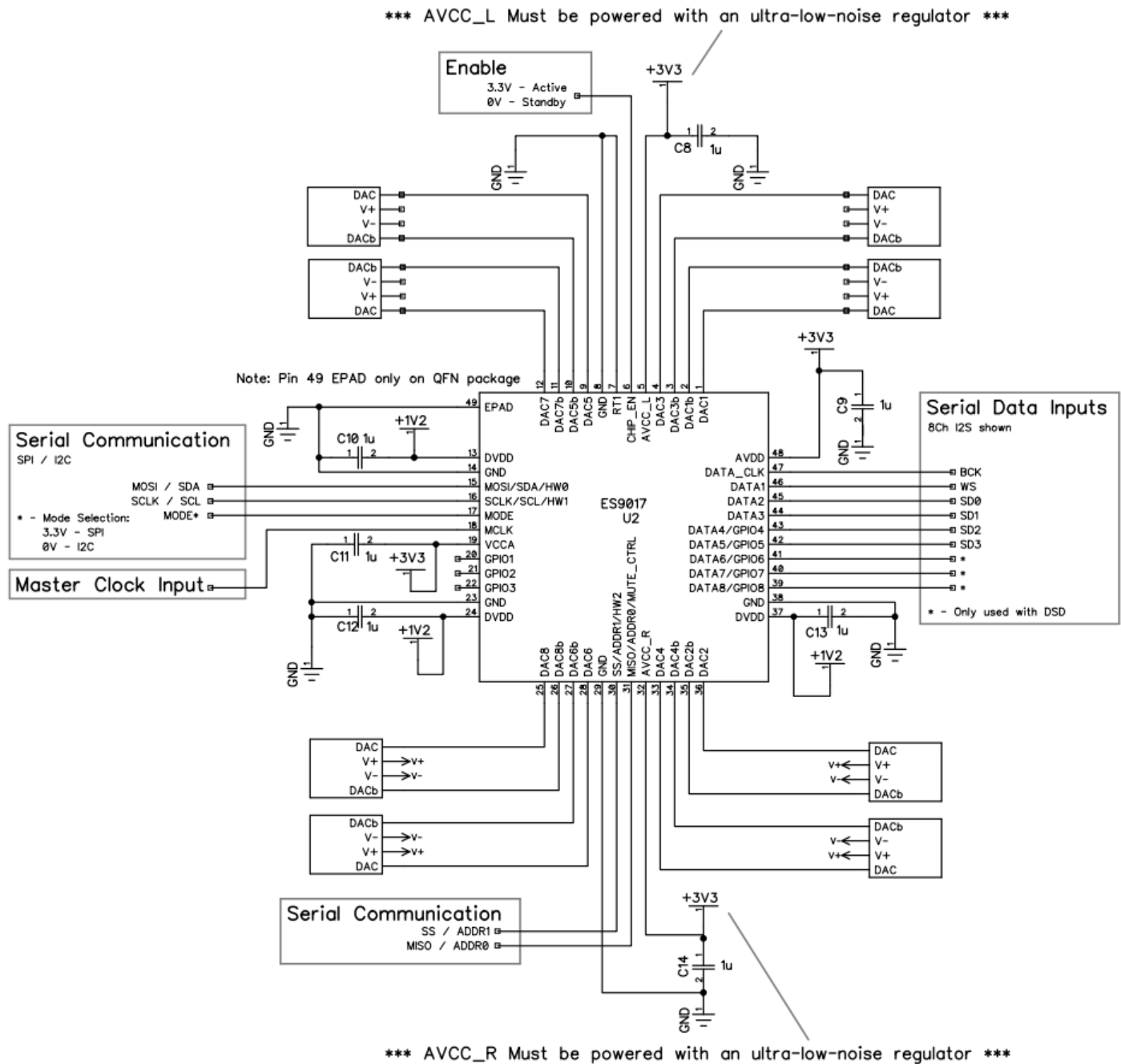


Figure 16 – Software mode reference schematic for ES9017Q

Note: ES9017Q has an exposed pad (EPAD, pin 49) and should be connected to ground. ES9017S does not have an exposed pad.

### Recommended Output stage

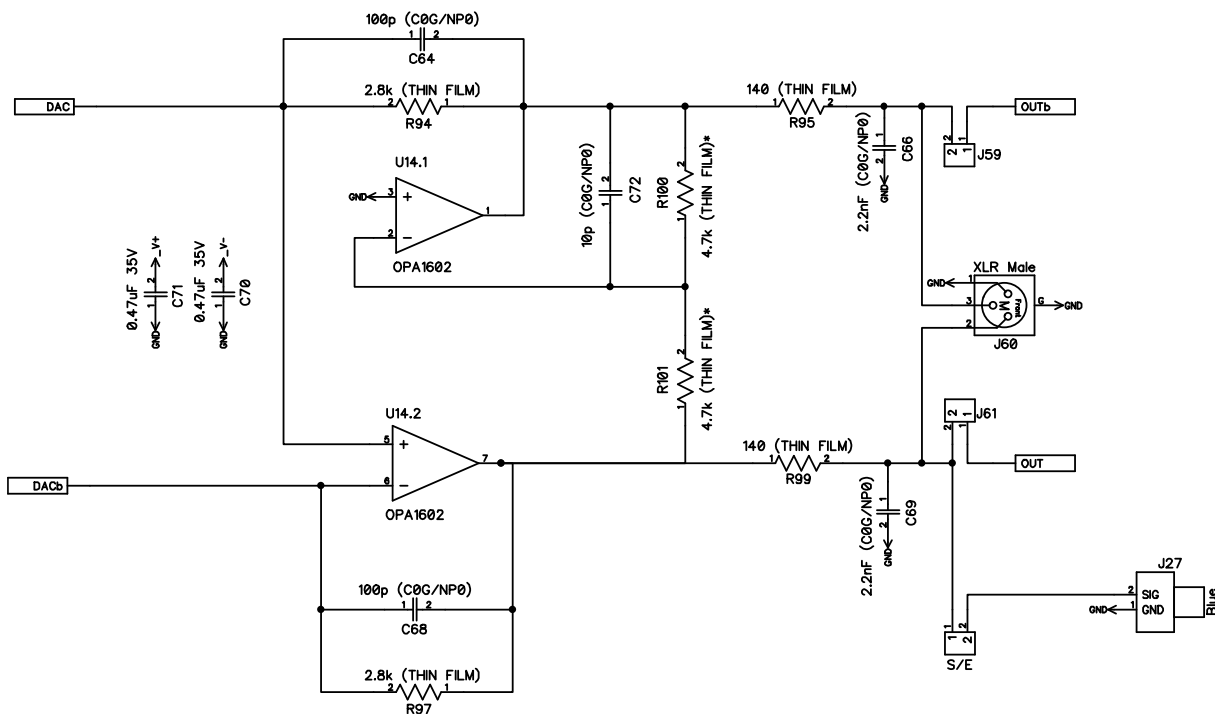
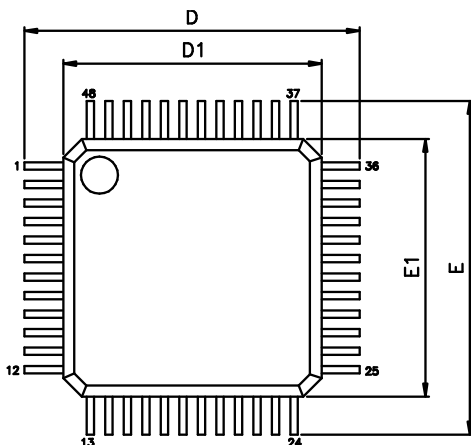


Figure 14 – Output stage schematic for ES9017Q

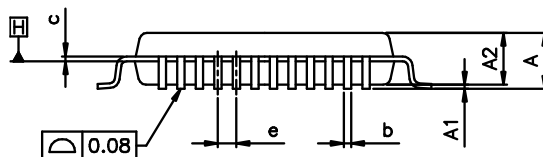
Note: Schematic is representative of ES9017 EVB v1.1.

### 48 QFP Package Dimensions



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
$\theta$	0°	3.5°	7°



NOTES:

1. JEDEC OUTLINE : MS-026 BBC
2. DATUM PLANE [A] IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE [A].
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

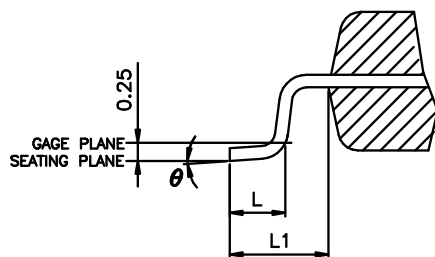


Figure 17 – ES9017S 48 QFP package dimensions

### 48 QFN Package Dimensions

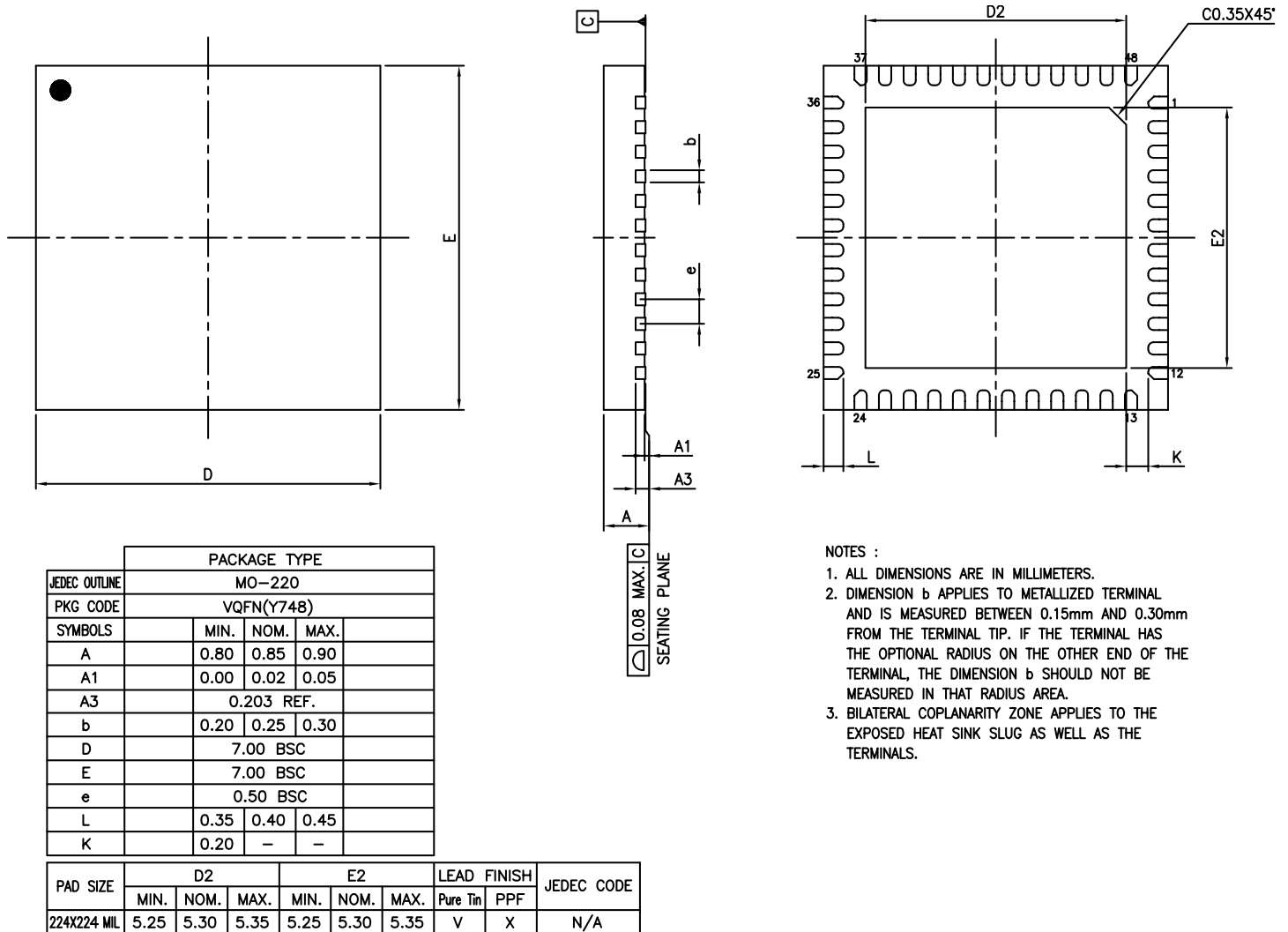


Figure 18 – ES9017Q 48 QFN package dimensions

### 48 QFP Top View Marking

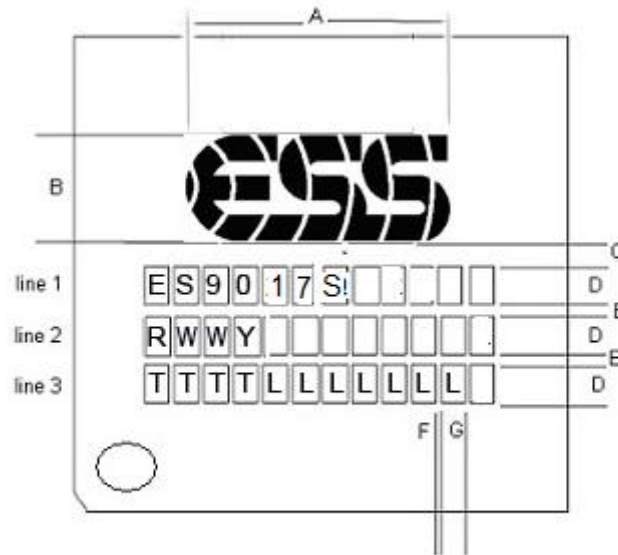


Figure 19 – ES9017S Marking

Package Type	Dimension in mm						
	A	B	C	D	E	F	G
48 LQFP 7mm x 7mm	5.0	2.0	0.3	0.56	0.2	0.08	0.33

<i>T</i>	<i>Tracking number</i>
<i>W</i>	<i>Work week</i>
<i>Y</i>	<i>Last digit of year</i>
<i>L</i>	<i>Lot number</i>
<i>R</i>	<i>Silicon Revision</i>



### 48 QFN Top View Marking

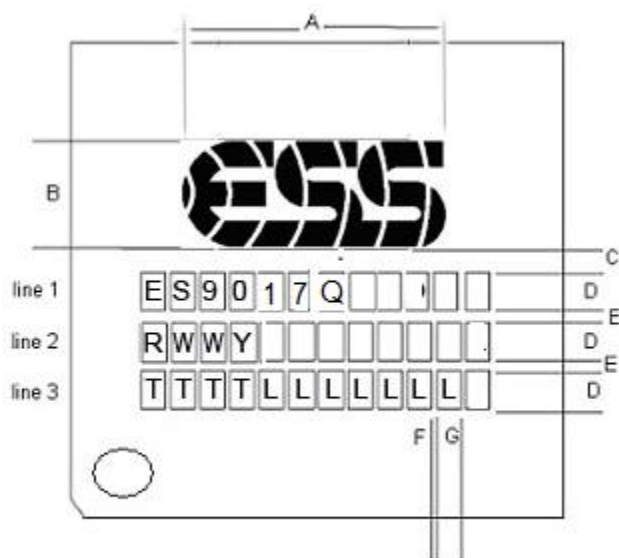


Figure 20 – ES9017Q Marking

Package Type	Dimension in mm						
	A	B	C	D	E	F	G
48 QFN 7mm x 7mm	5.0	2.0	0.3	0.56	0.2	0.08	0.33

<i>T</i>	<i>Tracking number</i>
<i>W</i>	<i>Work week</i>
<i>Y</i>	<i>Last digit of year</i>
<i>L</i>	<i>Lot number</i>
<i>R</i>	<i>Silicon Revision</i>



## Reflow Process Considerations

### Temperature Controlled

For lead-free soldering, the characterization and optimization of the reflow process is the most important factor to consider.

The lead-free alloy solder has a melting point of 217°C. This alloy requires a minimum reflow temperature of 235°C to ensure good wetting. The maximum reflow temperature is in the 245°C to 260°C range, depending on the package size ([RPC-2 Pb-Free Process – Classification Temperatures \(T<sub>c</sub>\)](#)). This narrows the process window for lead-free soldering to 10°C to 20°C.

The increase in peak reflow temperature in combination with the narrow process window makes the development of an optimal reflow profile a critical factor for ensuring a successful lead-free assembly process. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of the components, the mix of large and small components, and the paste chemistry being used. Reflow profiling needs to be performed by attaching calibrated thermocouples well adhered to the device as well as other critical locations on the board to ensure that all components are heated to temperatures above the minimum reflow temperatures and that smaller components do not exceed the maximum temperature limits (Table RPC-2).

To ensure that all packages can be successfully and reliably assembled, the reflow profiles studied and recommended by ESS are based on the JEDEC/IPC standard J-STD-020 revision D.1.

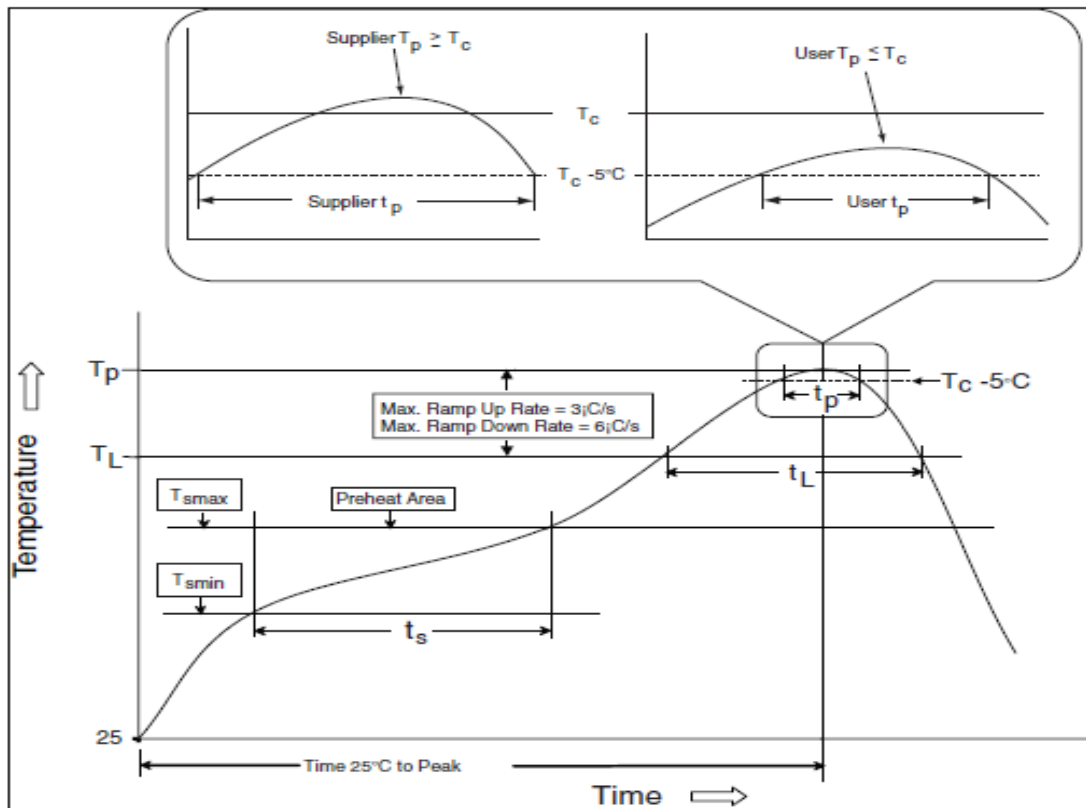


Figure 21 – IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)

Reflow is allowed 3 times. Caution must be taken to ensure time between re-flow runs does not exceed the allowed time by the moisture sensitivity label. If the time elapsed between the re-flows exceeds the moisture sensitivity time bake the board according to the moisture sensitivity label instructions.

### Manual

Allowed up to 2 times with maximum temperature of 350°C no longer than 3 seconds.



## RPC-1 Classification reflow profile

Profile Feature	Pb-Free Assembly
<b>Preheat/Soak</b>	
Temperature Min (T <sub>sm</sub> )	150°C
Temperature Max (T <sub>sm</sub> )	200°C
Time (ts) from (T <sub>sm</sub> to T <sub>sm</sub> )	60-120 seconds
Ramp-up rate (TL to T <sub>p</sub> )	3°C / second maximum
Liquidous temperature (TL)	217°C
Time (t <sub>L</sub> ) maintained above TL	60-150 seconds
Peak package body temperature (T <sub>p</sub> )	For users T <sub>p</sub> must not exceed the classification temp in Table RPC-2. For suppliers T <sub>p</sub> must equal or exceed the Classification temp in Table RPC-2.
Time (t <sub>p</sub> )* within 5°C of the specified classification temperature (T <sub>c</sub> )	30* seconds
Ramp-down rate (T <sub>p</sub> to TL)	6°C / second maximum
Time 25°C to peak temperature	8 minutes maximum
* Tolerance for peak profile temperature (T <sub>p</sub> ) is defined as a supplier minimum and a user maximum.	

Table 18 – RPC-1 Classification reflow profile

All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), T<sub>p</sub> shall be within ±2°C of the live-bug T<sub>p</sub> and still meet the T<sub>c</sub> requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures, refer to JEP140 for recommended thermocouple use.

Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table RPC-1.

*For example, if T<sub>c</sub> is 260°C and time t<sub>p</sub> is 30 seconds, this means the following for the supplier and the user.*

*For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.*

*For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.*

All components in the test load shall meet the classification profile requirements.

## RPC-2 Pb-Free Process – Classification Temperatures (T<sub>c</sub>)

Package Thickness	Volume mm <sup>3</sup> , <350	Volume mm <sup>3</sup> , 350 to 2000	Volume mm <sup>3</sup> , >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Table 19 – RPC-2 Pb free classification temperatures

At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (T<sub>p</sub>) can exceed the values specified in Table RPC-2. The use of a higher T<sub>p</sub> does not change the classification temperature (T<sub>c</sub>).

Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.

The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

## Ordering Information

Part Number	Description	Package
ES9017S	High Performance SABRE 32-bit 8 Channel DAC	7mm x 7mm 48 QFP
ES9017Q <ul style="list-style-type: none"> <li>Inquire for availability</li> </ul>		7mm x 7mm 48 QFN

## Revision History

Current Version 0.2

Rev.	Date	Notes
0.1	June 24, 2022	Initial release
0.2	December 20 <sup>th</sup> , 2022	<ul style="list-style-type: none"> <li>Unreserved Register 54[2:0]</li> <li>Updated Register 2[7], 24-23[15] descriptions</li> <li>Updated HW mode pin configurations table, ES9017 is a synchronous device only</li> <li>Changed labeling of MSB Justified to Left Justified in HW table</li> <li>Added Timing Requirements section, I2C Slave Timing section title</li> <li>Reserved Register 55[2]</li> <li>Corrected ramp_rate equations in Register 48-50</li> <li>Updated Register 2[2] description</li> <li>Added soft ramp equation Register 63[4:0]</li> <li>Updated ESD protection</li> <li>Updated Audio Inputs Formats section</li> <li>Added note for TDM_CHx_LINE_SEL "Note: Valid for TDM, PCM and DoP"</li> <li>Changed register description for TDM_CHx_LINE_SEL</li> <li>Reference to register overview section corrected</li> <li>Added missing SPI commands to SPI section</li> <li>Added recommended output stage schematic</li> <li>Added Hardware mode schematics</li> <li>Updated Digital Signal Path diagram</li> </ul>

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