PRODUCT / PROCESS CHANGE NOTIFICATION
PCN-000614
Date: APR-28-2021

Semtech Corporation, 200 Flynn Road, Camarillo CA 93012

Change Details

Part Number(s) Affected:	**Customer Part Number(s) Affected:** ☐ N/A
GN24L80-WP GN24L80-GRP6 GN24L80-GRP6UV	

Description, Purpose and Effect of Change:

1. To allow Intel to order GN24L80 die, in sawn quarter-wafer format on GRP6, with the tape on the GRP6 placed on UV-sensitive tape, a new order code has been added to the device datasheet (GN24L80-GRP6UV). To order GRP6 on tape that is *not* UV sensitive, order code GN24L80-GRP6 should be used.

2. To better align the expected device performance with possible manufacturing variation, the maximum Tz gain values have been changed/increased. No changes to minimum or typical values are expected, and these values remain unchanged in the data sheet.

Change Classification	☐ **Major** ☒ **Minor**	**Impact to Form, Fit, Function**	☐ **Yes** ☒ **No**
Impact to Data Sheet	☒ **Yes** ☐ **No**	**New Revision or Date**	**Rev. 7** ☐ **N/A**

Impact to Performance, Characteristics or Reliability:

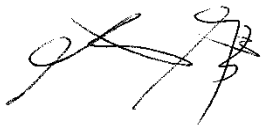
No change in device characteristics or reliability is expected. Over manufacturing variation, the maximum differential transimpedance of the device may be higher than indicated in version 6 of the GN24L80 datasheet.

Implementation Date	**May-28-2021**	**Work Week**	**21**
Last Time Ship (LTS) **Of unchanged product**	**N/A**	**Affecting Lot No. / Serial No. (SN)**	**N/A**
Sample Availability	**N/A**	**Qualification Report Availability**	**N/A**

Supporting Documents for Change Validation/Attachments:

- PDS-061025 Rev. 7 (see following pages)

Issuing Authority

Semtech Business Unit:	Signal Integrity Product Group (SIP)	
Semtech Contact Info:	Pedro Jr. Bernas Quality Assurance pbernas@semtech.com (289) 856-9326 x1162	

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High Sensitivity CMOS TIA for Time of Flight Measurement Applications

Main Features

- High dynamic range
- Single +3.3V power supply
- Typical power dissipation of 116mW
- Maximum Transimpedance: 80kΩ (typical)
- Differential CML data outputs
- Photodiode current monitor output
- Ambient light cancellation system
- Programmable transimpedance settings
- Programmable low-frequency cut-off
- Compatible with large area APD photo detectors with 1.55pF capacitance (typical)
- Pb-free/Halogen-free/RoHS & WEEE compliant

Applications

- Time of Flight Gesture Recognition
- 3D Cameras
- LiDAR (non-automotive)
- Optical Distance Measurement

General Description

The GN24L80 is a high-sensitivity Transimpedance Amplifier (TIA), manufactured in a low-cost pure CMOS process. The GN24L80 provides over 30dB of dynamic operating range and operates with large aperture photo detectors while maintaining a large bandwidth, resulting in a high-performance TIA designed for cost-sensitive applications where low power is essential.

Specifically designed to provide controlled latency, low-input referred noise and fast overload recovery, the GN24L80 enables Time Of Flight (TOF) measurement dependent systems.

Featuring a photodiode current monitor, an ambient light cancellation system, programmable transimpedance and low frequency cut-off settings, the GN24L80 offers a flexible, high-performance receiver solution for TOF applications.

The GN24L80 is supplied as bare die; available on GRP-6 quarter-wafers or in waffle packs.

This product is for use in non-automotive applications only.

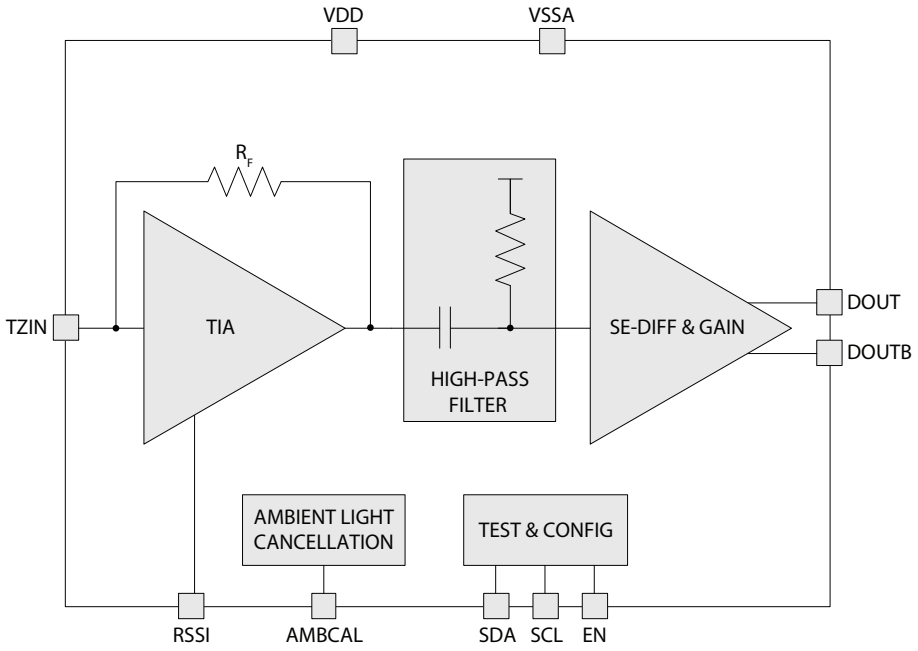


Figure A: GN24L80 Functional Block Diagram

Revision History

Version	ECO	PCN	Date	Changes and/or Modifications
7	050885	000614	March 2021	Updates to Main Features. Increased maximum values of differential transimpedance in Table 2-3: Electrical Characteristics. Added new part number for GN24L80 die on GRP6 and GRP6UV, with UV-sensitive tape in Table 7-1: Wafer Packing Label Key and Table 8-1: Ordering Information.
6	046615	000560	July 2019	Updates to Table 2-1: Absolute Maximum Ratings, Figure 7-1: Wafer on GRP-6 Ring Packing Label and Table 7-1: Wafer Packing Label Key.
5	038559	—	January 2019	Updates to Electrical Characteristics, Register Descriptions and Applications Information sections. Converted to Final status.
4	036124	—	April 2017	Update for Revision C00 of the GN24L80.
3	031069	—	May 2016	Update for Revision B00 of the GN24L80.
2	026380	—	November 2015	Reformatted document with latest corporate template.
1	026133	—	June 2015	New document.

Contents

1. Pad Out

1.1 Pad Assignment

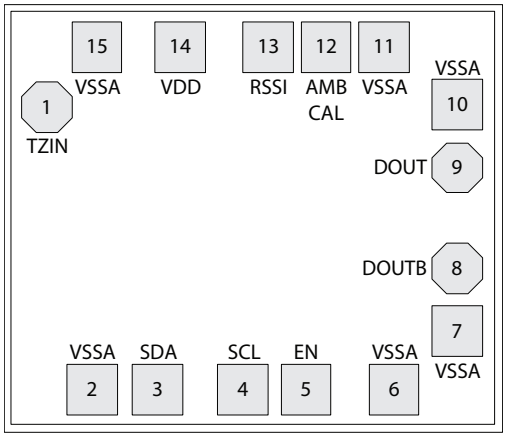


Figure 1-1: Pad Assignment

1.2 Pad Descriptions

Table 1-1: Pad Descriptions

Pad	Name	Description
1	TZIN	Signal input. Connection to APD Cathode.
2	VSSA	Supply ground pad.
3	SDA	Serial Data, 1.8V.
4	SCL	Serial Clock, 1.8V.
5	EN	Device Enable; 1.8V = Enable, 0V = Disable. Internal pull-down to ground.
6	VSSA	Supply ground pad.
7	VSSA	Supply ground pad.
8	DOUTB	Inverting data output pad.
9	DOUT	Non-inverting data output pad.
10	VSSA	Supply ground pad.
11	VSSA	Supply ground pad.
12	AMBCAL	LV-CMOS input. Internal pull-down to ground.
13	RSSI	Received Signal Strength Indicator monitor output. Sources current.
14	VDD	Positive supply connection for the IC.
15	VSSA	Supply ground pad.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

These are the absolute maximum ratings beyond which the IC can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not implied.

Parameter	Value / Units
Power Supply (V_{DD})	-0.5V to +3.8V
Storage Temperature (T_{STG})	-65°C to +150°C
Maximum Junction Temperature (T_J)	+125°C
Maximum DC TZIN Input Current ($I_{INMAX-DC}$)	1mA
Maximum Pulsed TZIN Input Current ($I_{INMAX-PULSE}$), for a maximum pulse width of 700ns	50mA[1]
HBM Model; all pins except for TZIN (ESD)	2kV
Maximum Slew Rate of ramp-up of VAPD supply (SRV_{APD})	No requirement
Minimum delay between application of V_{DD} settling and application of V_{APD} (power-up) (t_V_{APDR})	>0µs
Minimum delay between removal of V_{DD} and removal of V_{APD} (power-down) (t_V_{APDF})	No requirement—V_{APD} can remain asserted. See Section 3.1.

Notes:

1. The pulsed current refers to current sourced from the TZIN pin, through the APD, to the negative APD bias supply, V_{APD}.

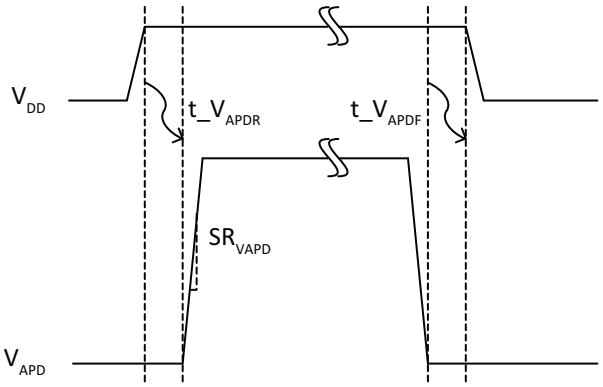


Figure 2-1: Timing of V_{APD} vs V_{DD}

2.2 Recommended Operating Conditions

Table 2-2: Recommended Operating Conditions

Symbol	Parameter	Rating	Units
V_{DD}	Power Supply Voltage (V_{DD} to GND)	3.14 to 3.46	V
T_{die}	Operating Temperature[1]	0 to +65	°C
C_{PD}	Photodiode Capacitance	1.55	pF
IBW_{APD}	Intrinsic APD Bandwidth (-3dB point)	850	MHz
R_{LOAD}	Differential Output Loading	100	Ω

Notes:

1. I^2C Read/Write functionality guaranteed from -10°C to +65°C.

2.3 Electrical Characteristics

Over recommended operating conditions. Typical values are at V_{DD} = 3.3V and T_{die} = 25°C.

Table 2-3: Electrical Characteristics

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Photodiode TZIN Voltage		V_{TZIN}	0.59	0.63	0.67	V	1
Supply Current	Mission Mode: EN = 1.8V	I_{DD}	—	35	44	mA	—
	Power Down: EN = 0V		—	20	28	µA	—
	Power Down via I^2C: EN = 1.8V, **PWD** = '1'		—	360	462	µA	—
	Power Down, Digital Core ON: EN = 0V, **EN_PIN_MODE** = '1'		—	200	300	µA	—
Input Characteristics							
Linear Dynamic Range Upper Limit		I_{INLIN}	8	—	—	$µA_{pp}$	—
Saturation Dynamic Range Upper Limit		I_{INSAT}	100	—	—	$µA_{pp}$	—
Overload dynamic range upper limit		I_{INOLD}	1	—	—	mA_{pp}	—

Table 2-3: Electrical Characteristics (Continued)

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Transition effect; recovery between saturation and linear range	**SIGPATH_LFC** = "00"	T_{trans}	—	100	160	ns	2
	SIGPATH_LFC = "01"		—	150	230	ns	
	SIGPATH_LFC = "10"		—	500	700	ns	
	SIGPATH_LFC = "11"		—	2.33	4.00	µs	
Input referred noise density	1MHz to 850MHz	$I_{NOISE-INT}$	—	5.1	5.7	pA/rHz	3
	at 250MHz	$I_{NOISE-250}$	—	3.0	—	pA/rHz	
	at 500MHz	$I_{NOISE-500}$	—	4.8	—	pA/rHz	
Output referred noise	**GAIN_TRIM** = "00"	O_{NOISE}	—	11.9	15.6	mV_{RMS}	4
Output Characteristics							
Single-ended output impedance		R_{OUT}	—	50	—	Ω	5
Low-frequency cut-off	**SIGPATH_LFC** = "00"	LFC	—	8	—	MHz	6
	SIGPATH_LFC = "01"		—	4	—	MHz	
	SIGPATH_LFC = "10"		—	1	—	MHz	
	SIGPATH_LFC = "11"		—	125	—	kHz	
Differential transimpedance	**GAIN_TRIM** = "00", T = 0°C	G_{TOT}	70	82	100	kΩ	7
	GAIN_TRIM = "00", T = 25°C		69	77	92	kΩ	
	GAIN_TRIM = "00", T = 65°C		61	70	81	kΩ	
	GAIN_TRIM = "01", T = 0°C		57	64	80	kΩ	
	GAIN_TRIM = "01", T = 25°C		54	60	72	kΩ	
	GAIN_TRIM = "01", T = 65°C		49	53	64	kΩ	
	GAIN_TRIM = "10", T = 0°C		39	44	55	kΩ	
	GAIN_TRIM = "10", T = 25°C		36	41	50	kΩ	
	GAIN_TRIM = "10", T = 65°C		33	37	43	kΩ	
	GAIN_TRIM = "11", T = 0°C		26	29	42	kΩ	
	GAIN_TRIM = "11", T = 25°C		24	27	33	kΩ	
	GAIN_TRIM = "11", T = 65°C		22	24	30	kΩ	
Differential Transimpedance Temperature Coefficient	**GAIN_TRIM** = "00"	$TC\text{-}G_{TOT}$	-0.30	-0.20	-0.12	kΩ/°C	8
	GAIN_TRIM = "01"		-0.22	-0.16	-0.10		
	GAIN_TRIM = "10"		-0.14	-0.11	-0.07		
	GAIN_TRIM = "11"		-0.09	-0.07	-0.05		
Optical Bandwidth to -3dB point	Over linear operating range	BW	733	850	—	MHz	9
Maximum differential output voltage		V_{DIFF}	600	700	800	mV_{pp}	—
Common mode output voltage		V_{CM}	—	1.45	—	V	10
Voltage dependent propagation delay (wrt ΔV_{DD})		T_{PROPV}	—	0.34	0.5	ps/mV	11

Table 2-3: Electrical Characteristics (Continued)

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Temperature dependent propagation delay		T_{PROPT}	—	0.58	0.66	ps/°C	11
Input level dependent propagation delay		T_{PROPI}	—	5	10	ps/dec	11
Duty Cycle Distortion		DCD	—	0	20	ps	12
Data Dependent jitter		DDJ	—	11.7	30	ps_{pp}	12
Random Jitter		RJ	—	—	50	ps_{RMS}	12
Power Supply Rejection Ratio		PSRR	12	14	—	dB	13
Control and Monitoring							
Input current range over which the RSSI current is linear		I_{RSSI}	5.0	—	1000	µA	14
Uncalibrated RSSI accuracy; percentage error	$5µA < I_{RSSI} < 12µA$ $12µA < I_{RSSI} < 100µA$ $100µA < I_{RSSI} < 1000µA$	Acc_{RSSI}	-25 -15 -8	3 2 1	25 15 8	% % %	—
Calibrated RSSI accuracy; percentage error	$5µA < I_{RSSI} < 100µA$	$ACC\text{-}CAL_{RSSI}$	-10	—	10	%	15
RSSI Gain Slope	$5µA < CAL\text{-}I_{RSSI} < 100µA$	$GAIN_{RSSI}$	0.9	—	1.1	—	16
RSSI timing	$5µA < I_{RSSI} < 12µA$ $12µA < I_{RSSI} < 100µA$ $100µA < I_{RSSI} < 1000µA$	T_{RSSI}	— — —	— — —	11 11 12	µs µs µs	17
MON compliance		V_{COMP}	—	—	1	V	18
Enable pin de-assert time (disabling the device)		T_{ENDEAS}	—	—	1	µs	19
Enable pin assert time (enabling the device)		T_{ENASS}	—	60	100	µs	20

Table 2-3: Electrical Characteristics (Continued)

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Maximum DC-level current able to compensate for		I_{AMB}	105	127	—	µA	—

Notes:

1. Measured with 0A input current.
2. Measured with step current from $50\mu A_{pp}$ to $1\mu A_{pp}$ with 80kΩ gain setting; up to first single-ended data crossing. 820pF AC-coupling capacitors at the TIA outputs.
3. Noise density from 1MHz to 850MHz calculated using trapezoidal rule integration. Calculated by IRN (f) = ORN (f) / Gain (f). Resolution bandwidth = 51kHz.
4. Measured with **GAIN_TRIM** = "00", in dark conditions, C_{PD} = 1.55pF, Intrinsic APD Bandwidth = 700MHz assuming 1st order roll-off, M = 100, 6.8nH input-peaking inductor, 1nH equivalent APD cathode to TZIN pad bond-wire inductance. An ideal 938MHz 4th order Bessel-Thompson filter is applied. AMBCAL is disabled.
5. Measured differentially across data outputs. The measured value is then halved.
6. $I_{IN} = 2.5\mu A_{av}$, T = 25°C.
7. Measured electrically at 50MHz in the TIA linear region using 3-port Network Analyser S-parameters.
8. Slope coefficients are on a per-device basis and are not derived from Min/Typ/Max Gain values.
9. Bandwidth -3dB point, relative to 50MHz, measured at $I_{IN} = 2.5\mu A_{av}$, C_{PD} = 1.55pF, Intrinsic APD Bandwidth = 700MHz assuming 1st order roll-off, M=100, 6.8nH input-peaking inductor, 1nH equivalent APD cathode to TZIN pad bond-wire inductance.
10. Measured DC using a high-impedance voltmeter.
11. Guaranteed by design.
12. Maximum value measured at 50µA average input photo-current. DCD and DDJ typical values are based on worst-case simulated values at $I_{IN} = 1\mu A_{pp}$.
13. Measured $\Delta V_{OUT}/\Delta V_{DD}$, with supply decoupling, from 1MHz to 10MHz. For further pin filtering, see the Applications Information section.
14. Average photodiode current.
15. Calibration procedure is to measure I_{RSSI} at input currents of 5µA & 10µA, then subtract 2 x I_{RSSI} @ 5µA, from I_{RSSI} @ 10µA, and store the result as an offset current, subtracting this from subsequent I_{RSSI} readings. The values shown assume calibration is done once the device is at room temperature and V_{DD} = 3.3V. Calibrated accuracy includes supply voltage and temperature variation.
16. Slope defined as Δ CAL-$I_{RSSI}/\Delta I_{IN}$, where 5µA < CAL-I_{RSSI} < 100µA.
17. Measured with the RSSI output pin filtering enabled, **RSSI_FILT** = '1'.
18. Compliance voltage relative to V_{DD}.
19. From EN pin de-assertion to the last valid data transition at the output pins, measured with the LFC set to 1MHz and **EN_PIN_MODE** = '1'.
20. From EN = HIGH to DOUT/DOUTB reaching 90% of settled output swing, measured with the LFC set to 1MHz and **EN_PIN_MODE** = '1'.

2.4 AMBCAL Timing

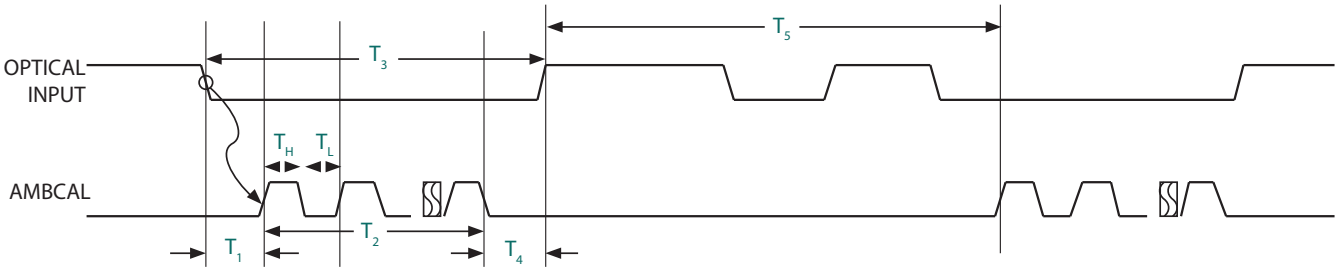


Figure 2-2: AMBCAL Timing

Table 2-4: AMBCAL Timing

	Min (µs)	Max (µs)	Description
T_1	2	—	Minimum time, T_1, before ambient light cancellation sequence can start after optical input ceases
T_2	8	2000	Calibration sequence width
T_3	12	—	Minimum total dark period required for calibration procedure to start and finish
T_4	2	—	Minimum settling period for ambient light cancellation procedure to complete before optical input resumes
T_5	10	—	Minimum period between the ambient light calibration
T_H	6	—	HIGH time of AMBCAL pulse
T_L	2	—	LOW time of AMBCAL pulse

2.5 Digital Interface Section Characteristics

Table 2-5: Digital Interface Section Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
Slave I²C Interface (1.8V)						
V_{IH}	HIGH Level input voltage (SDA, SCL)	1.17	—	—	V	—
V_{IL}	LOW Level input voltage (SDA, SCL)	—	—	0.63	V	—
V_{OH}	LOW Level output voltage (SDA, open-drain)	—	—	0.45	V	—
F_{SCL}	Maximum SCL Clock	—	400	—	kHz	1
t_{LOW}	Minimum LOW period of SCL clock	—	1.2	—	µs	—
t_{HIGH}	Minimum HIGH period of SCL clock	—	0.6	—	µs	—
t_{DH}	Minimum data hold time	—	0	—	ns	—
t_{DS}	Minimum data set-up time	—	100	—	ns	—
t_R	Maximum rise time for SDA and SCL	—	100	—	ns	—
t_F	Maximum fall time for SDA and SCL	—	100	—	ns	—
t_{SS}	Minimum set up for STOP condition	—	0.6	—	µs	—
t_{BUF}	Minimum bus free time between a STOP and START condition	—	1.2	—	µs	—
$C_{I/O}$	Maximum capacitance for each I/O pin	—	10	—	pF	—
Low Speed I/O: EN, AMBCAL pins						
V_{IH}	Input voltage HIGH	1.17	—	—	V	2
V_{IL}	Input voltage LOW	—	—	0.63	V	2

Notes:

1. I²C Slave interface operates at 100kHz and 400kHz without any clock stretching.
2. Guaranteed by design.

3. Detailed Description

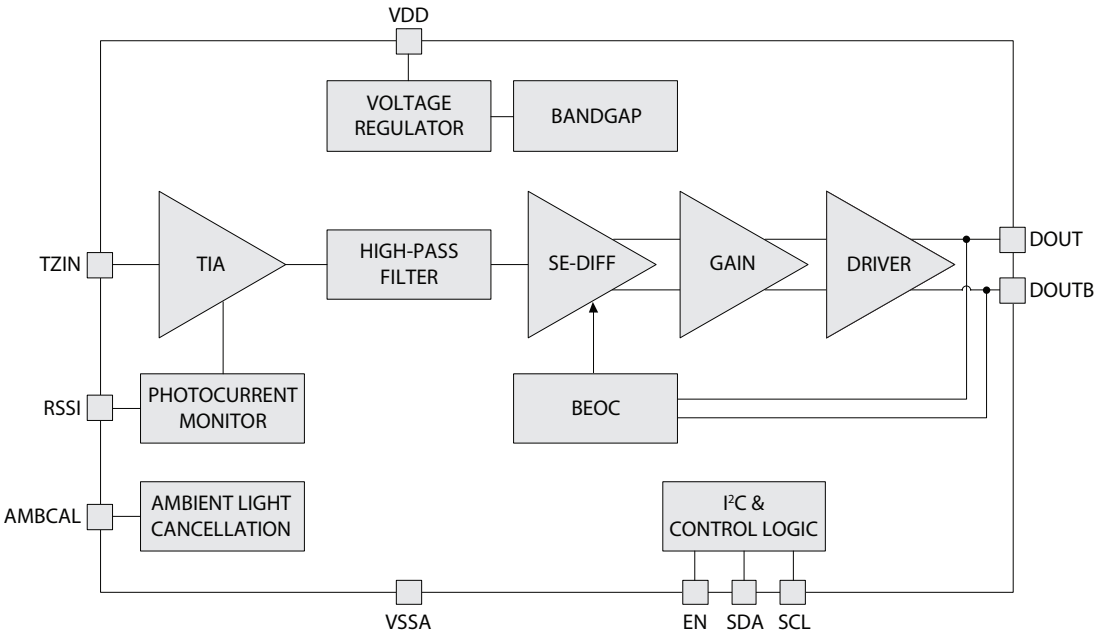


Figure 3-1: Detailed Block Diagram

The GN24L80 comprises an AC-coupled multi-stage amplifier which contains a transimpedance amplifier stage, a single-ended to differential converter with offset control, a limiting amplifier stage, an output buffer and DC-restore circuit.

The TIA features a photo current monitor output, *RSSI*, that sources a copy of the photodiode current. The RSSI current is derived from the TZIN input current.

3.1 Power Sequencing and Power-down

The GN24L80 operates from a single 3.3V (typical) power supply. As the APD is externally biased with a high negative voltage (V_{APD}), it is necessary to follow the correct power sequence and ramp in order to prevent damage to the pin connected to the APD (*TZIN*). This should follow the timing and sequence as illustrated in Figure 2-1.

The GN24L80 can be fully powered-down by deasserting the *EN* pin (EN = 0V), when register **EN_PIN_MODE** = 0. Setting register **EN_PIN_MODE** = 1 changes the functionality of the *EN* pin when EN = 0V to "soft power-down" mode; internal regulators and digital functionality remain powered, allowing fast power-up due to the registers retaining their previously set values.

Alternatively, writing register **PWD** = 1, also powers down the chip while retaining digital register values, but allows the *EN* pin to remain asserted (EN = 1.8V). Normal chip operation can be restored by writing **PWD** = 0. During power-down using the *EN* pin or **PWD** register, it is safe to keep V_{APD} applied.

3.2 TIA, Gain and HPF Stages

The transimpedance stage features a CMOS low-noise amplifier with integrated feedback resistor. The operational range is split into three sections:

- **Linear:** there is no memory effect between received pulses
- **Saturated:** there is some memory effect between received pulses, but there is fast recovery when the received power is in the linear range again
- **Overload:** operation without damage

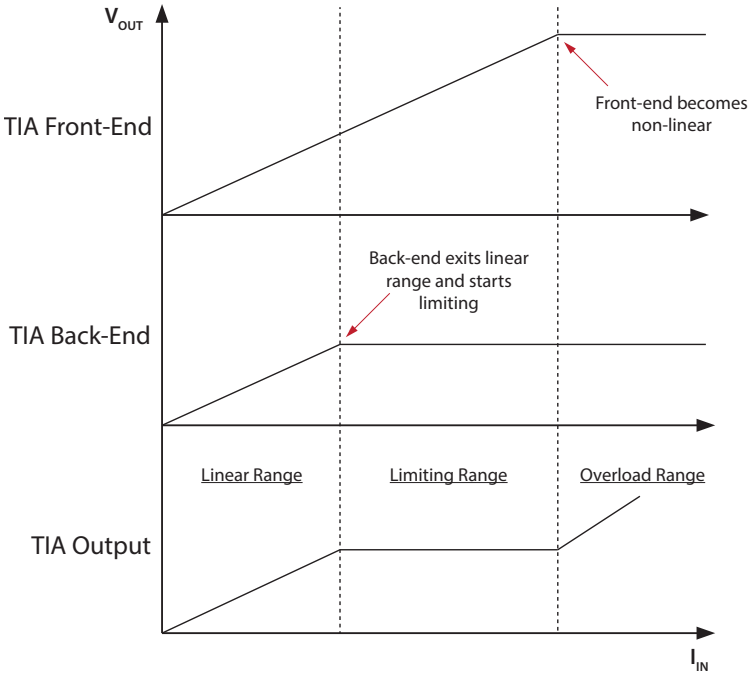


Figure 3-2: TIA Operating Ranges

The TIA gain created via the internal feedback resistor is a fixed value, however the overall system gain can be controlled digitally via the **GAIN_TRIM** registers.

Table 3-1: Gain Control Settings

Register 02_h[1:0]	Gain (kΩ)
00	80
01	60
10	40
11	26

The gain control sets the slope of the linear region, as shown below.

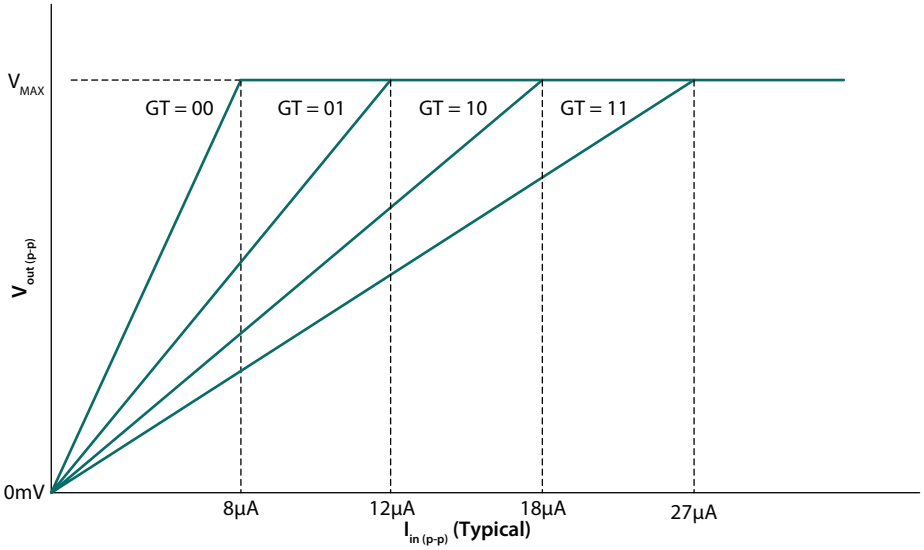


Figure 3-3: Gain Control Function

The TIA stage is AC-coupled to the further stages of the signal path. This forms a High-Pass Filter (HPF) which is programmable to allow control of the system Low-Frequency Cut-off (LFC).

Table 3-2: LFC Control Settings

Register 04_h[1:0]	LFC (MHz)
00	8
01	4
10	1
11	0.125

3.3 SE-to-Differential and Output Driver Stages

The GN24L80 output stage combines a phase splitter with a driver stage to convert the single-ended signal from the transimpedance front end into a differential voltage output. The CML output driver has single ended 50Ω terminations and is designed to drive a differential 100Ω load via AC-coupling capacitors. The output is capable of driving capacitive loads.

3.4 Ambient Light Cancellation (AMBCAL)

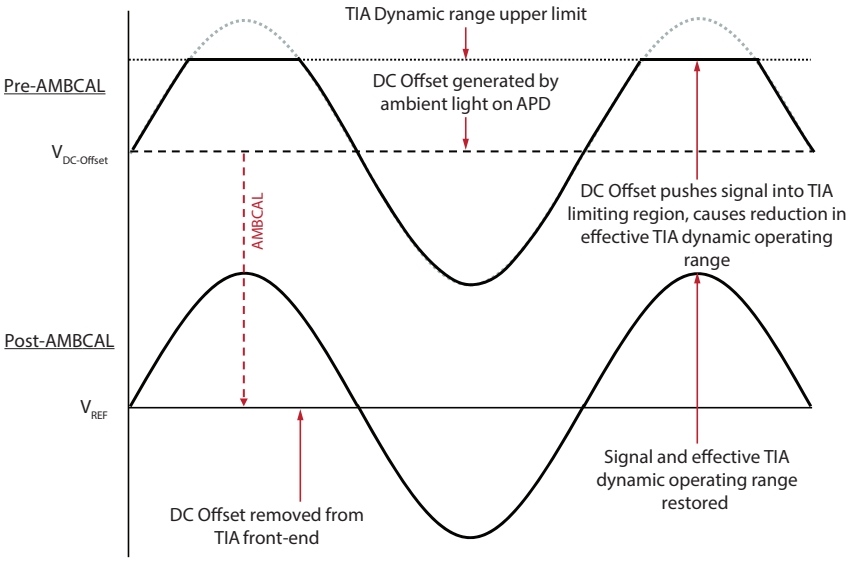


Figure 3-4: AMBCAL Function on TIA Front-end Output, before the High-Pass Filter

For optimal operation of the GN24L80 in high ambient light conditions, the device provides Ambient Light Cancellation (AMBCAL) capability. This can recover the TIA's dynamic range which is normally compromised by the presence of ambient light. The AMBCAL system is most effective when the TIA front-end, which is where the system is implemented, is no longer in its linear region. See Figure 3-2 for more information on TIA operating regions.

During the AMBCAL procedure, the host must ensure that laser sources have been shut-down, or that any input photo current into the TIA originates solely from ambient light. This measure is crucial in order to take full advantage of the AMBCAL feature to allow recovery of the full dynamic operating range and avoid overcompensation.

Operating the AMBCAL system requires the host to provide a pulse with a period of 8µs to the *AMBCAL* pin using the timing specification described in Section 2.4. Various cancellation step sizes can be configured to provide slower convergence with higher accuracy (small step size) or faster convergence with lower accuracy (larger step size); 1µA, 2µA, 4µA, and 8µA. The step size can be controlled by configuring the **STEP_SIZE** register.

One pulse will provide one step-size worth of cancellation, therefore it is likely that multiple pulses will be required to cancel out all of the present ambient light photo current. There is no maximum time requirement between consecutive pulses, meaning that the device will hold the last accumulated cancellation value from the last received pulse.

AMBCAL operates in a closed-loop fashion with the RSSI circuit. It compares against the RSSI current value to converge on the correct level of cancellation required. A current comparator in the AMBCAL system uses a known internal reference current to distinguish when the AMBCAL correction current is higher or lower than the ambient light level, and therefore will cause the system to either decrement or increment the correction current by one step-size on the next AMBCAL pulse. As the AMBCAL system converges, the measured RSSI current value approaches 0A. Therefore, any residual current generated from the inherent inaccuracy of the RSSI circuit will not be significant enough to impact the TIA front-end operation. The system cannot overcompensate if the *AMBCAL* pin is continuously pulsed after the cancellation target has already been reached. There must be no "wanted signal" current present with the ambient light current during the AMBCAL procedure, because it uses the RSSI current as a convergence target.

If the level of ambient light drops from the quantity at which the system was calibrated for, the signal will start to clip from the bottom relative to the reference voltage the signal it's swinging around. There is a margin of no more than 3µA of which the actual ambient light can vary down from the compensated value before any clipping may occur. In the case of large levels of overcompensation due to significant ambient light level reductions, the TIA front-end will effectively become heavily attenuated or even appear to be squelched.

The AMBCAL procedure should therefore be run at regular intervals, especially in an environment with dynamic ambient light levels to avoid situations of over-compensation resulting in signal clipping.

The AMBCAL system can be disabled via the **AMB_DIS** register.

The GN24L80 can be configured to subtract the compensated ambient light current from the total input photo current, which is mirrored onto the *RSSI* pin. See Section 3.5 for details.

3.5 Photodiode Current Monitor

The *RSSI* output provides a copy of the mean photodiode input current on *TZIN* via a current mirror.

When the AMBCAL system is enabled and after the AMBCAL procedure has been completed, the current on the *RSSI* pin represents the sum of the ambient light induced current and the received signal current.

The current induced by ambient light can be subtracted from the RSSI measurement reading by writing register **AMBSUB** = 1, leaving only the received signal current.

The *RSSI* output can be used to provide Overload detection, and used as an input to an Analogue-to-Digital Converter (ADC) for system diagnostic applications.

The RSSI output is configured as a current source with reference to V_{DD}. By connecting a resistor between the RSSI output and ground (GND), a voltage proportional to the photodiode current can be generated and used as an input to an ADC. See Figure .

RSSI functionality can be enabled or disabled via the **RSSI_EN** register. Disabling RSSI functionality reduces chip current consumption. The output can also be filtered through a 300kHz (typical) bandwidth low-pass filter by setting register **RSSI_FILT** = 1.

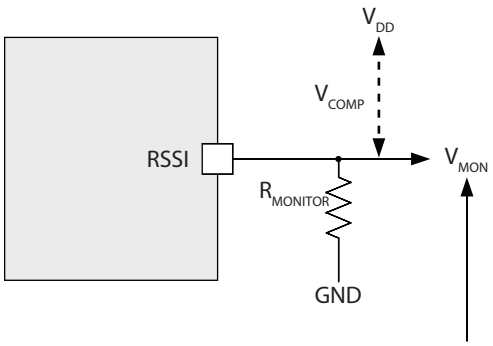


Figure 3-5: RSSI Sourcing

3.6 Digital Control & Monitoring Features

The GN24L80 is set-up, programmed and controlled via an I^2C digital interface. Registers in the GN24L80 are used to control the various analogue functions within the IC. The GN24L80 registers can be found at I^2C address $6C_h$.

3.6.1 Digital I^2C Interface

The I^2C interface is a slave interface responding to read and write requests from an external master interface on a host controller. The SDA and SCL interface lines require external pull-up resistors to be fitted. The interface supports the standard 100kHz mode and 400kHz fast mode.

An I^2C transaction is contained within a frame that is preceded by a start condition and completed by a stop condition. A start condition is defined by the host master pulling the SDA line LOW while the SCL line is HIGH. A stop condition is defined by the host master releasing the SDA to transition LOW-to-HIGH while the SCL line remains HIGH.

The master interface has control of the bus during a framed transaction. The GN24L80 allows repeat start conditions in which the master may send multiple frames delimited by a start condition before finally sending a stop condition. This allows the master to send multiple frames without releasing control of the bus.

During a framed data transaction, data is transferred from master to slave or slave to master by clocking data on the bus. A data bit is valid during a clock LOW-to-HIGH transition while the SDA state may only change when the SCL line is LOW. Data is arranged as 8 bits followed by an acknowledge (ACK) bit. The acknowledge bit is controlled by the recipient of the data by holding the SDA line LOW to acknowledge the correct receipt of a data byte. A not-acknowledged (NACK) bit can be signalled by leaving the SDA line floating during the 9th SCL clock cycle. A not-acknowledge can be used to indicate several conditions depending on the nature of the transaction and data content.

3.6.2 Address Decoding

After a start condition from the master indicates the beginning of a frame, the master must then send an address byte to the slave. The address byte is formatted as shown in Figure 3-6. The first seven bits contain the address of the target slave device with the MSB first. The eighth bit indicates the type of transaction required: a '0' indicates a write (master writes to slave) and a '1' indicates a read (master reads from slave). If no slave on the bus matches the address sent, then the SDA line will be left floating and therefore the master receives a NACK back. The master must then send a stop condition.

If a slave does appear on the bus with the target address then it must pull down the SDA line thus sending an acknowledge back to the master at which point communication between master and slave can proceed depending on the type of transaction requested—write or read.

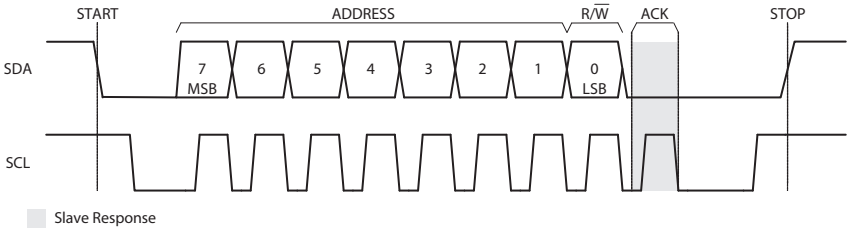


Figure 3-6: I²C Address Decoding

3.6.3 Write Transaction

A write transaction is shown below in Figure 3-7. Communication is initiated by the host master driving the I²C bus with a start condition. The host master then signals the 7-bit slave (GN24L80) address followed by a write bit, indicating that the host master intends to write data to the slave. The slave then acknowledges the master by holding down the SDA line (shown in grey). The host master then proceeds to write data on to the bus, 8-bits wide with MSB first, and then receives an acknowledge from the slave (again, in grey). The diagram below shows the first byte of data and acknowledge followed by a stop condition.

BYTE WRITE: A single byte write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the GN24L80 will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the GN24L80 will output a zero and the host master device must terminate the write sequence with a stop condition.

PAGE WRITE: The GN24L80 is capable of an 8-byte page write. A page write is initiated the same as a byte write, but the host master does not send a stop condition after the first data word is clocked in. Instead, after the GN24L80 acknowledges receipt of the first data word, the host master can transmit up to seven data words. The GN24L80 will respond with a zero after each data word received.

The data word address lower three bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than eight data words are transmitted to the GN24L80, the data word address will "page wrap" and previous data will be overwritten.

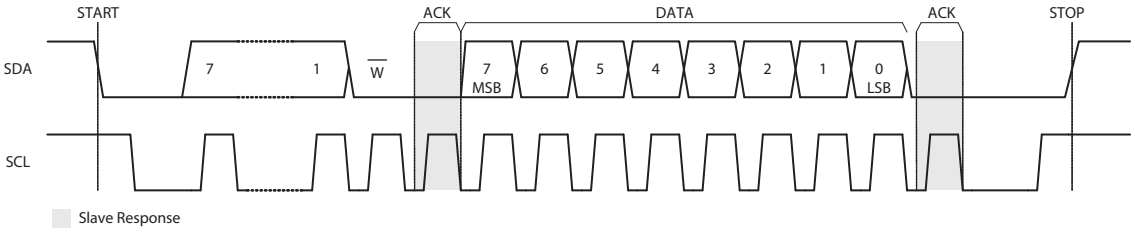


Figure 3-7: I²C Write Transaction

3.6.4 Read Transaction

Figure 3-8 below shows a read transaction. The master sends the slave address followed by a read request bit which is subsequently acknowledged by the slave (the first grey bit). The slave then responds by placing data onto the bus (shown in grey) from the current memory location held in the register address pointer. The master will then hold down the SDA line to acknowledge (shown in white) the successful receipt of the data byte. The process can continue until the master terminates the communication with a stop condition.

To read data from random register addresses the master must first send write to the slave followed by the register address to be read from and a stop condition. The master can then initiate a read frame and the slave will read out consecutive data bytes starting from the register address indicated in the previous write frame.

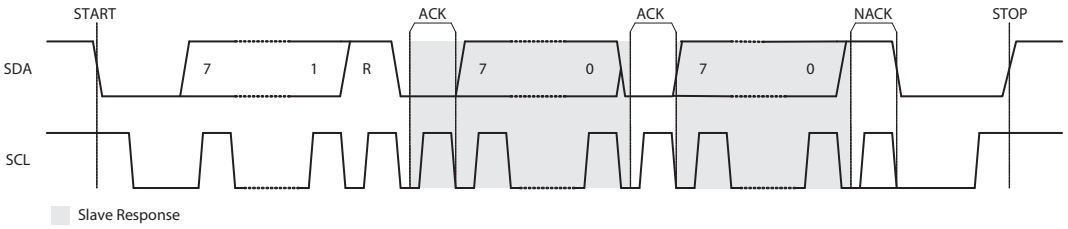


Figure 3-8: I²C Read Transaction

3.6.5 Slave I²C Time-out/Recovery

Incorrect operation of the slave I²C interface to the GN24L80 can result in unintended behaviour. This unintended behaviour would be the result of a break in normal communications with the GN24L80 device mid-access. The unintended behaviour could manifest itself by the GN24L80 possibly holding the SDA signal LOW as it was in the process of clocking out data when the break in communications happened. This could result in the next access to the GN24L80 failing.

The GN24L80 has built-in protection that can be enabled to ensure that the slave I²C interface will recover automatically if a break in communications occurs during mid-transaction with the GN24L80.

If the user does not want to use the internal protection then a simple recovery sequence can be sent to the GN24L80 device to recover its I²C interface and ensure that any subsequent access will succeed. The two options are detailed below.

1. If the host sets the **I2C_TIMEOUT_EN** bit then the GN24L80 will monitor for when it is driving the SDA signal LOW. If the GN24L80 drives the SDA signal LOW for more than 10 SCL clock periods, the GN24L80 will reset its slave I²C interface. Once this time-out has occurred the GN24L80 will release its control of the SDA signal and go back to the idle state.
2. If the host does not want to use the time-out functionality then a simple recovery sequence can be sent to the GN24L80 device to recover its slave I²C interface. The sequence to be sent by the host is to send 9 consecutive STOP conditions. Once sent the host can then resume normal communications with the GN24L80.

4. Register Descriptions

The GN24L80 registers are located at I^2C address $6C_h$.

Table 4-1: Register Descriptions

00	**00_h**		**RESERVED**	**Reserved**
Bit	**R/W**	**PoR**		
7:0	—	FF_h	Reserved	—
01	**01_h**		**OP_MODES1**	**Status & Control**
Bit	**R/W**	**PoR**		
7:6	—	00	Reserved	—
5	R/W	0	RSSI_FILT	Selects RSSI filtering mode (0 = unfiltered, 1 = filtered). When enabled, a 300kHz (typical) bandwidth low-pass filter is applied to the RSSI output.
4	—	0	Reserved	—
3	R/W	0	AMBSUB	Subtract ambient light current from RSSI output (0 = current included, 1 = current subtracted)
2	R/W	1	RSSI_EN	Enables RSSI function (0 = RSSI disabled, 1 = RSSI enabled)
1	R/W	0	RX_INVERT	Data output polarity (0 = normal, 1 = inverted)
0	R/W	0	PWD	Power-down the TIA, digital core remains active (0 = TIA powered up, 1 = TIA powered down)
02	**02_h**		**TRIM_CODES**	**Status & Control**
Bit	**R/W**	**PoR**		
7:4	—	00_h	Reserved	—
3:2	R/W	0	Reserved	—
1:0	R/W	11	GAIN_TRIM	Change total gain. See Table 3-1 for value details.
03	**03_h**		**RESERVED**	**Reserved**
Bit	**R/W**	**PoR**		
7:0	R/W	00_h	Reserved	—
04	**04_h**		**LFC**	**Status & Control**
Bit	**R/W**	**PoR**		
7:2	—	00_h	Reserved	—
1:0	R/W	00	SIGPATH_LFC	Cut-off frequency for HPF in signal path. See Table 3-2 for value details.

Table 4-1: Register Descriptions (Continued)

05	05_h		AMBCODE	Status & Control
Bit	**R/W**	**PoR**		
7	—	0	Reserved	—
6:0	R	00_h	AMBCODE	Ambient light cancellation DAC code
06	**06_h**		**AMBCAL**	**Status & Control**
Bit	**R/W**	**PoR**		
7:4	—	00_h	Reserved	—
3	R/W	0	AMB_DIS	Disable the ambient light cancellation function (0 = AMBCAL enabled, 1 = AMBCAL disabled)
2	R/W	0	Reserved	—
1:0	R/W	00	STEP_SIZE	Adjust the ambient light cancellation response time
07	**07_h**		**RESERVED**	**Reserved**
Bit	**R/W**	**PoR**		
7:4	—	00_h	Reserved	—
3:0	R/W	$0F_h$	Reserved	—
08	**08_h**		**OP_MODES_2**	**Status & Control**
Bit	**R/W**	**PoR**		
7:6	R/W	00_h	Reserved	—
5	R/W	0	CHIP_SETUP_5	Set to '0'
4	R/W	0	CHIP_SETUP_4	Set to '1'
3	R/W	0	CHIP_SETUP_3	Set to '1'
2	R/W	0	CHIP_SETUP_2	Set to '0'
1	R/W	0	CHIP_SETUP_1	Set to '0'
0	R/W	0	CHIP_SETUP_0	Set to '1'
09	**09_h**		**OP_MODES_3**	**Status & Control**
Bit	**R/W**	**PoR**		
7:5	R/W	000_h	Reserved	—
4	R/W	0	CHIP_SETUP_4	Set to '1'
3	R/W	0	CHIP_SETUP_3	Set to '1'
2	R/W	0	CHIP_SETUP_2	Set to '0'
1	R/W	0	CHIP_SETUP_1	Set to '1'
0	R/W	0	CHIP_SETUP_0	Set to '0'

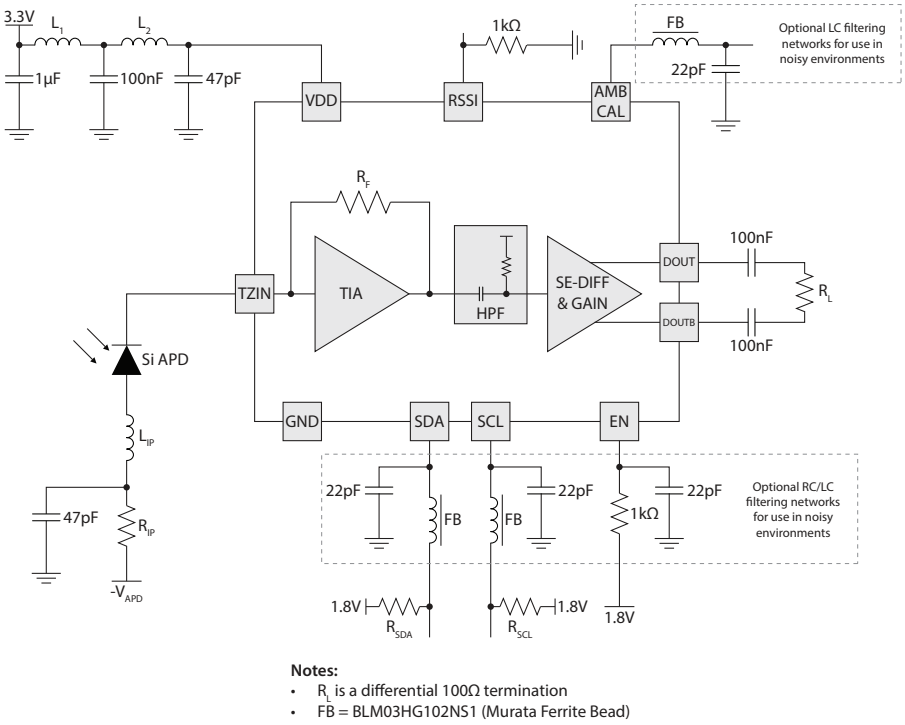
Table 4-1: Register Descriptions (Continued)

10	A_h		OP_MODES_4	Status & Control
Bit	**R/W**	**PoR**		
7:2	R/W	00_h	Reserved	—
1	R/W	0	CHIP_SETUP	Set to '1'
0	R/W	0	EN_PIN_MODE	EN de-assert functionality (0 = full power-down, 1 = soft power-down and digital core remains active)
11 to 21	**B_h to 15_h**		**RESERVED**	**Reserved**
Bit	**R/W**	**PoR**		
7:0	—	FF_h	Reserved	—
22	**16_h**		**RESERVED**	**Reserved**
Bit	**R/W**	**PoR**		
7:1	—	00_h	Reserved	—
0	R/W	0	Reserved	—
23	**17_h**		**RESERVED**	**Reserved**
Bit	**R/W**	**PoR**		
7:0	R/W	00_h	Reserved	—
24	**18_h**		**I2C_SETUP**	**Status & Control**
Bit	**R/W**	**PoR**		
7:3	—	00_h	Reserved	—
2	R/W	0	I2C_TIMEOUT_EN	Built-in time-out recovery. If the slave pulls SDA LOW for more than 10 SCL clock periods. (0 = recovery disabled, 1 = recovery enabled)
1	R/W	1	Reserved	—
0	R/W	0	Reserved	—

Table 4-1: Register Descriptions (Continued)

25 to 37	19_h to 25_h		CHIPNAME	Status & Control
Bit	R/W	PoR		
7:0	R	47_h	CHIPNAME_0	G
7:0	R	$4E_h$	CHIPNAME_1	N
7:0	R	32_h	CHIPNAME_2	2
7:0	R	34_h	CHIPNAME_3	4
7:0	R	$4C_h$	CHIPNAME_4	L
7:0	R	38_h	CHIPNAME_5	8
7:0	R	30_h	CHIPNAME_6	0
7:0	R	$2D_h$	CHIPNAME_7	—
7:0	R	43_h	CHIPNAME_8	C
7:0	R	30_h	CHIPNAME_9	0
7:0	R	$2D_h$	CHIPNAME_10	—
7:0	R	30_h	CHIPNAME_11	0
7:0	R	30_h	CHIPNAME_12	0

5. Applications Information



Notes:
- R_L is a differential 100Ω termination
- FB = BLM03HG102NS1 (Murata Ferrite Bead)

Figure 5-1: Typical Application Circuit

The applications circuit shown in Figure 5-1 features a negatively-biased APD at the input of the TIA, with input-peaking to boost system bandwidth via inductor L_{IP}. In a typical system, with an APD Cathode to TZIN pad bond-wire inductance of approximately 1nH, the recommend value for L_{IP} = 6.8nH. System bandwidth is dependent on the sum of these inductances as well as the APD terminal capacitance, C_T. Using an APD with a C_T greater than the typical of 1.55pF will result in a reduction of system bandwidth and a likely-hood of increased noise in the system.

A series resistor, R_{IP}, should be added to create a high-impedance AC open-circuit, to restrict the AC current path through the 47pF bypass capacitor on the high-voltage APD bias trace. The recommended value for R_{IP} = 10Ω. The capacitor should be positioned on the PCB to create a short current loop back to the nearest *GND* pin on the TIA.

It is recommend that generous amounts noise filtering should be provided for VDD on the PCB via bypass capacitors using values suggested in Figure 5-1, which should be positioned to have as short as possible current loops from the *VDD* pin to the adjacent *GND* pin on-chip.

Additional filtering for the I/O pins can be also be added, as shown in Figure 5-1, if the TIA is being utilized in a noisy system or environment. Devices such as laser drivers and DC-DC converters can produce high-frequency, high-magnitude noise which can propagate across PCBs and/or free-space, and then couple to I/O traces. Placing the filtering components as close the TIA pins as possible will aid in shielding the TIA from the noise. Component values may need to be modified to tailor to the frequency and magnitude of the noise present in the system or environment.

External pull-up resistors are required to be fitted on *SDA* and *SCL* traces for the I^2C interface to function correctly. The I^2C interface can be driven via 1.8V and 3.3V host interfaces, however 1.8V interfaces are preferred.

All *GND* pads should be connected to ground via wire-bonds, and that they should be as short as possible. For further wire-bonding guidance, contact Semtech Applications support.

6. Die Information

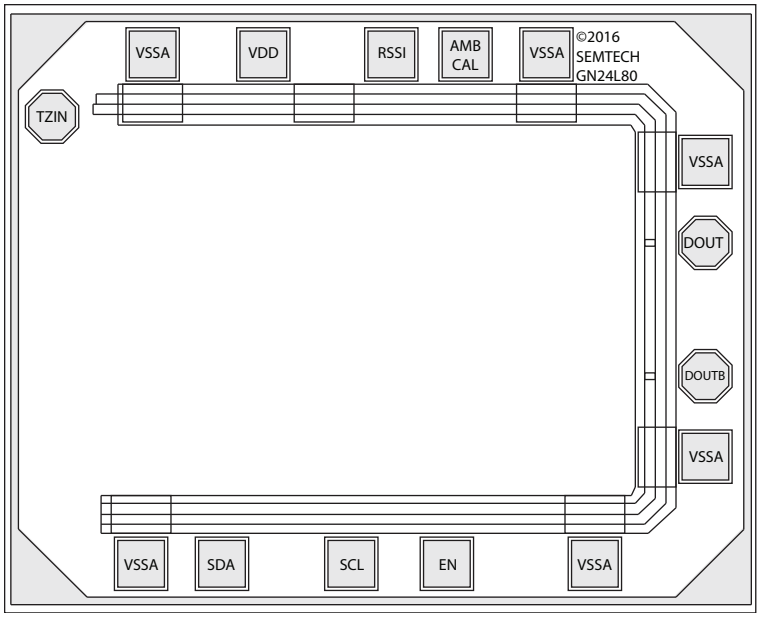


Figure 6-1: Mechanical Die Drawing (Top View)

Nominal Die Size:	1000µm x 800µm (excluding scribe lane)
Sawn Die Size—x: Sawn Die Size—y:	1010µm (minimum) to 1070µm (maximum) 810µm (minimum) to 870µm (maximum)
Scribe Line:	80µm
Nominal Pad Size:	60µm (passivation opening)
Die Thickness:	275µm ± 10%
Die Passivation:	Silicon Nitride

Table 6-1: GN24L80 Pad Locations

Pad Name	#	Pad Function	Pad Position (µm, centre 0,0)	Pad Size (µm)
TZIN	1	Signal input. Connection to APD Cathode.	-445, 261	60x60 (octagonal)
VSSA	2	Supply ground pad.	-325, -345	60x60
SDA	3	Serial Data.	-215, -345	60x60
SCL	4	Serial Clock.	-40, -345	60x60
EN	5	Device enable; 1.8V = Enable, 0V = Disable. Internal pull-down to ground.	90, -345	60x60
VSSA	6	Supply ground pad.	290, -345	60x60
VSSA	7	Supply ground pad.	440, -200	60x60
DOUTB	8	Inverting data output pad.	440, -90	60x60 (octagonal)
DOUT	9	Non-inverting data output pad.	440, 90	60x60 (octagonal)
VSSA	10	Supply ground pad.	440, 200	60x60
VSSA	11	Supply ground pad.	225, 345	60x60
AMBCAL	12	LV-CMOS input. Internal pull-down to ground.	115, 345	60x60
RSSI	13	Received Signal Strength Indicator monitor output. Sources current.	15, 345	60x60
VDD33	14	Positive supply connection for IC.	-160, 345	60x60
VSSA	15	Supply ground pad.	-310, 345	60x60

7. Wafer Information

One 8" wafer is supplied on four individually sawn and expanded GRP-6 wafer rings. Wafers include devices which have either passed or failed wafer-level testing. Failed parts are inked for visual indication. See Section 7.2 for inking information.

7.1 Wafer Packing Label

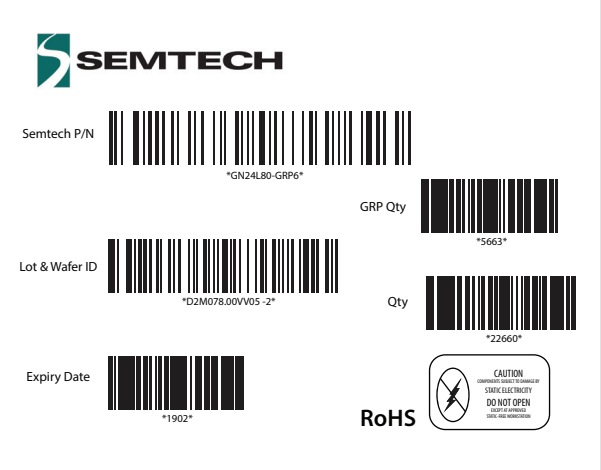


Figure 7-1: Wafer on GRP-6 Ring Packing Label

Table 7-1: Wafer Packing Label Key

Designator	Description
Semtech P/N	Semtech product part number *GN24L80-GRP6* or *GN24L80-GRP6UV*
Lot & Wafer ID & wafer quarter number	Foundry lot number and wafer identification number *LOT.WAFER-ID – quarter number* Key to wafer quarter numbers: 4 = upper left, 3 = upper right 1 = lower left, 2 = lower right
Expiry Date	Wafer expiry date *YYMM*
GRP Qty	Die quantity on GRP-6 quarter wafer *XXXX*
Qty	Die quantity on full 8" wafer *XXXXX*

7.2 Die Inking Specification

Each wafer includes die which has either passed or failed wafer-level testing. Die which have failed testing are ink marked to the following specification:

Ink Type: 6993-10mil or 6993-15mil

Ink Size: 300µm to 800µm

Ink Bake: 100°C for 20 minutes

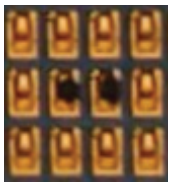


Figure 7-2: Inked (2pcs) and Non-Inked (10pcs) Die on GRP-6 Ring

Note: Die shown here may not represent actual GN24L80 die dimensions and are for illustrative purposes only.

7.3 Wafer Rings

7.3.1 Internal Ring

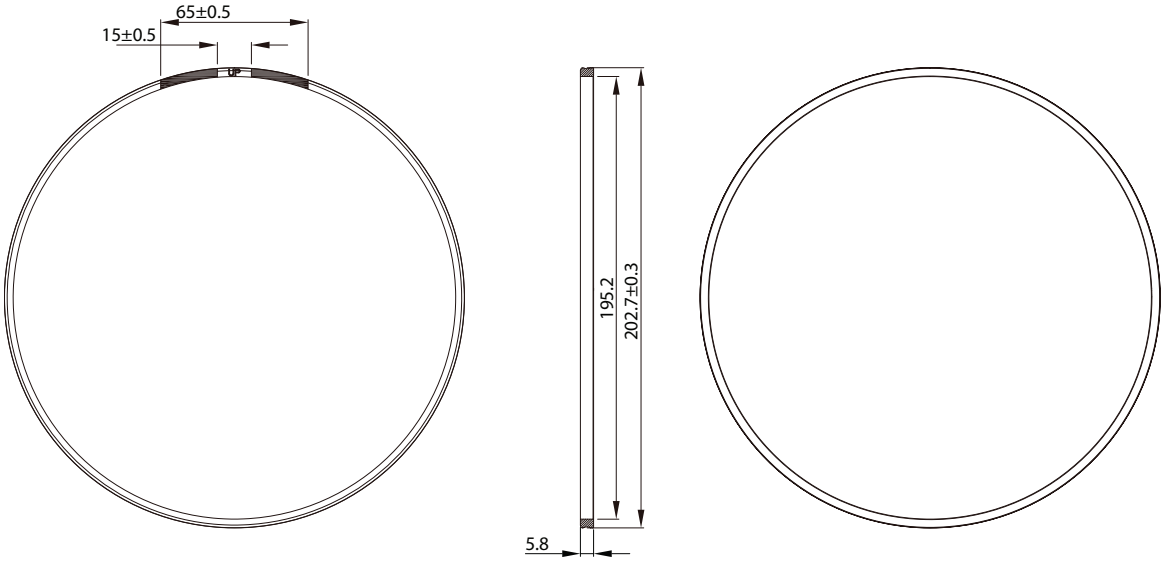
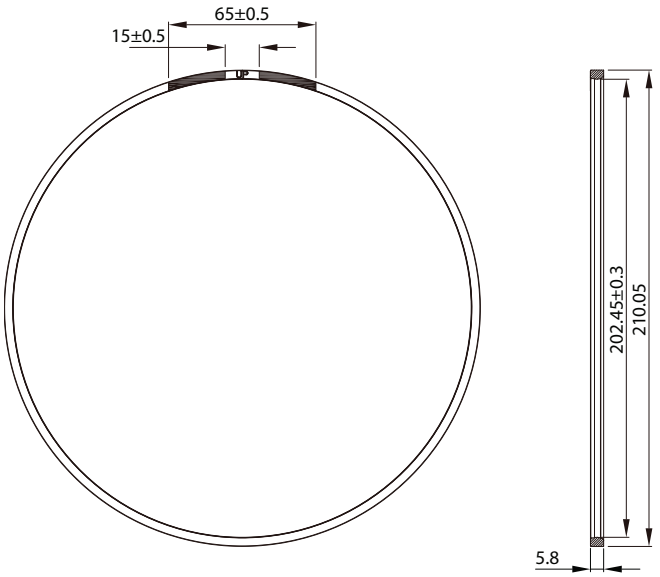


Figure 7-3: GRP-6, 6" Polycarbonate Wafer Ring—Internal Ring

7.3.2 External Ring



Dimensions in mm **Front View** **Side View**

Figure 7-4: GRP-6, 6" Polycarbonate Wafer Ring—External Ring

8. Ordering Information

Table 8-1: Ordering Information

Part Number	Package	Description
GN24L80-WP	Waffle Pack	500pcs in a standard waffle pack.
GN24L80-GRP6	Wafer	One 8" wafer is supplied on 4x individually sawn and expanded GRP-6 wafer rings. Die are attached to SPV-224 non-UV tape.
GN24L80-GRP6UV	Wafer	One 8" wafer is supplied on 4x individually sawn and expanded GRP-6 wafer rings. Die are attached to Adwill D-176 UV tape.

Contact Information

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